A Reconfigurable Prototyping Platform for Modern Communication Systems

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***Abstract*—The increasing number of upcoming communication systems make a reconfigurable platform concept inevitable. A strict modular, software-defined radio based concept allows to interchange several components in hardware as well as in software without affecting the residual parts of the platform in order to adapt the underlying system to various modern communication systems. In this paper, the authors describe a reconfigurable prototyping platform developed and successfully tested at the Department of Communication Technologies at University of Duisburg-Essen strictly following this software-defined radio paradigm. Using the example of the upcoming terrestrial broadcasting standard, namely DVB-T2, the necessity of a hybrid platform concept is discussed, comprising of a digital signal processor on the one hand and field-programmable gate arrays on the other hand.**

***Keywords*-DSP (Digital Signal Processor), Digital Video Broadcasting, DVB-T2, FPGA (Field Programmable Gate Array), LDPC (Low-Density Parity-Check) Codes, Prototyping Platform, Software-Defined Radio**

I. INTRODUCTION

The introduction of new communication systems, such as DVB (Digital Video Broadcasting), is mostly led by the demand for higher data rates. In order to be able to meet the various requirements, a sophisticated platform concept has to be developed. Within this paper, the authors present a reconfigurable prototyping platform based on the software-defined radio (SDR) concept [1]. Reconfigurability in radio development is not a very new technique [2]. Already during the 1980s, reconfigurable receivers were developed for radio intelligence in the short wave range. However, reconfigurability became familiar to many radio developers with the publication of the special issues on software radios of the IEEE Communication Magazine [3], [4]. The author in [2] refer to a transceiver as a software radio (SR) if its communication functions are realized as programs running on a suitable processor. Based on the same hardware, different transmitter/receiver algorithms, which usually describe transmission standards, are implemented in software in a cost effective manner [5]. An SR transceiver comprises all the layers of a communication system, in particular the physical layer, usually abbreviated by PHY layer, and the medium access control layer, denoted by MAC layer. Initially, the idea of software-defined radio was of academic interest only. However, due to the technological progress, modern hardware components are capable of making use of this concept. With the goal of implementing one of the world's first DVB-T2 (Digital Video Broadcasting - Terrestrial) receivers, a prototyping platform was developed at the Department of Communication Technologies at the University of Duisburg-Essen, strictly following the software-defined radio approach. DVB-T2 is the successor of DVB-T which has established itself as the leading specification for terrestrial television broadcasting after being introduced in the 1990s. The increasing demand for HDTV (High-Definition Television) paved the way towards a renovation of DVB-T, which does not allow the transmission of high-definition video streams. The goal of DVB-T2 was a higher spectral efficiency by using more sophisticated forward error correction techniques on the one hand and higher order modulation on the other hand. In the meantime, the standardization of DVB-T2, which began in 2006, has been completed [6].

In the following, the key parameters specified in the DVB-T2 standard [6] are mentioned. DVB-T and DVB-T2 are both based on Orthogonal Frequency Division Multiplexing (OFDM). While DVB-T uses a gross number of 8192 points, the OFDM size in DVB-T2 is 32768 points. The modulation order for each subcarrier goes up to 256 QAM (Quadrature Amplitude Modulation) in DVB-T2. Furthermore, the underlying forward error correction scheme is considerably modified. While DVB-T employs a combination of Reed-Solomon codes and convolutional codes, DVB-T2 makes use of a concatenation of BCH (Bose Chaudhuri Hocquenghem) codes and LDPC (Low-Density Parity-Check) codes with a block length of 64800 bits. LDPC codes are used in several modern and upcoming communication systems such as IEEE 802.16e (WiMAX) because of their near Shannon limit performance on the one hand and their ability for parallelized implementation on the other hand. Nevertheless, the real-time implementation of the LDPC decoder is one of the most challenging aspects when implementing DVB-T2 receivers. The modulation scheme, the channel coding parameters and the number of OFDM subcarriers have to be flexibly adaptable in the receiver [7]. Table I gives a brief comparison between

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	DVB-T	DVB-T2
FEC	Convolutional code + Reed-Solomon code	LDPC code + BCH code
Code rates	1/2, 2/3, 3/4, 5/6, 7/8	1/2, 3/5, 2/3, 3/4, 4/5, 5/6
Modulation	QPSK, 16-QAM, 64-QAM	QPSK, 16-QAM, 64-QAM, 256-QAM
Guard intervals	1/4, 1/8, 1/16, 1/32	1/4, 19/256, 1/8, 19/128, 1/16, 1/32, 1/128
OFDM sizes	2048, 8192	1024, 2048, 4096, 8192, 16384, 32768

TABLE I
SYSTEM PARAMETERS FOR DVB-T AND DVB-T2

the system parameters of DVB-T and DVB-T2 [6] [8].

Meeting the aforementioned requirements as well as being able to adapt the system to other communication standards requires a thorough investigation of state-of-the-art hardware components. A design merely based on digital signal processors (DSPs) is not powerful enough the achieve the desired goals. Thus, authors of this paper developed a hybrid concept which relies on a digital signal processor on the one hand and on field-programmable gate arrays (FPGAs) on the other hand. Due to the consequent deployment of the software-defined radio paradigm, the developed prototyping platform is capable of implementing various modern communication standard such as DVB-T2 and is ideally suited for concept engineering in the field of wireless communications in general. This manuscript is organized as follows. After this brief introduction, Section II gives an overview over the concept of the reconfigurable prototyping platform, followed by implementation aspects of this platform in Section III. Finally, the performance of the prototyping platform is addressed in Section IV.

II. RECONFIGURABLE PROTOTYPING PLATFORM CONCEPT

Figure 1 shows the suggested reconfigurable DVB-T2 receiver architecture. It consists of a fixed-point DSP board, which does not only implement major parts of the signal processing, but is also responsible for the scheduling of all platform components, which is an essential prerequisite for a reliable real-time demonstrator functionality. A mixed-signal daughter card, which implements analog signal processing and data conversion, connects directly to the DSP. In order to fulfill even very complex forward error correction requirements, such as the LDPC codes in DVB-T2 with a block length of 64800, a Virtex-5 FPGA evaluation module (EVM) is connected to the DSP, acting as a hardware accelerator. Finally, the decoded data is transferred to a data sink. While the DSP board and the Virtex-5 evaluation module are commercially available, the mixed-signal daughter card was developed by the authors of this paper. Its concept is shown in Figure 2. It consists of a further daughter card containing the RF (Radio Frequency) front end. The mixed-signal daughter card shall be able to allow processing signals in various frequency bands. Therefore, an analog-to-digital converter with an integrated down-conversion unit and advanced filtering capabilities should be used. Using a analog-to-digital converter with an integrated down-conversion unit has the advantage that the incoming intermediate frequency signal can be down-converted digitally. In order to be suitable for several communication systems, the sampling rate of the analog-to-digital converter should be reasonably high. The output of the analog-to-digital converter is fed into a Xilinx Spartan-3 FPGA for further basic signal processing purposes, such as additional filtering and sampling rate decimation. Furthermore, it buffers the data for the DSP. For improved flexibility, the authors follow a strict modular concept. In case of technology advances in a specific field, the corresponding module - in this context the mixed-signal daughter card - can be easily replaced without affecting the residual system. The USB (Universal Serial Bus) interface shown in Figure 2 is designed for debug reasons only.

The core part of the prototyping platform shown in Figure 1 is a DSP board with a powerful Texas Instruments TMS320C6455 fixed-point DSP running at 1.2 GHz. The

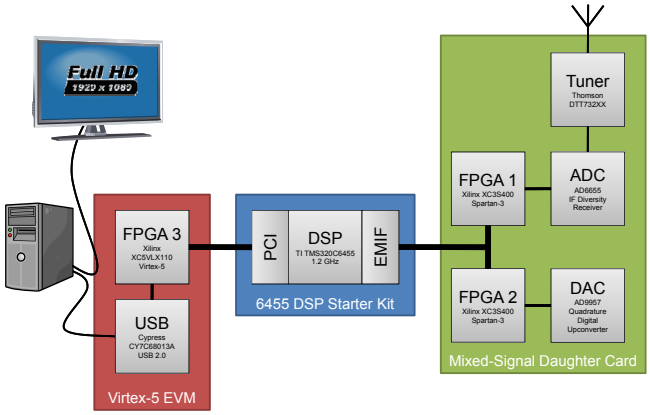

Fig. 1. Implementation concept of the SDR multimedia HDTV receiver

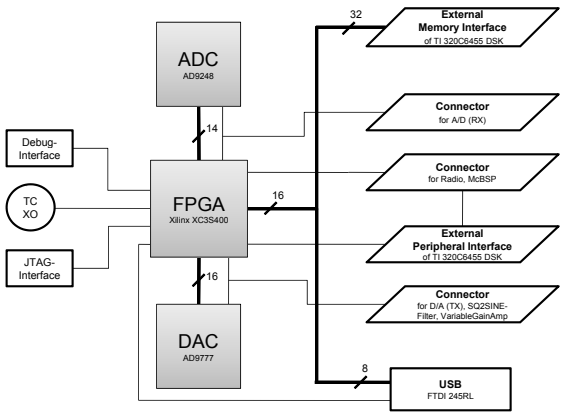

Fig. 2. Implementation concept of the mixed-signal daughter card

mixed-signal daughter card described before is connected to the DSP using a TI proprietary solution, namely the EMIF (External Memory Interface). In case of using the hardware accelerator for channel decoding, as it is done for the DVB-T2 implementation, the interface between the DSP and the Virtex-5 FPGA hardware accelerator demands for a reasonable high data rate depending on the resolution of the log-likelihood ratios representing the soft information for the channel decoder. This log-likelihood ratios are typically computed within the digital signal processor. This hardware accelerator for the DSP, which is also depicted in Figure 1, is implemented using an Avnet evaluation module hosting a Xilinx Virtex-5 LX110 FPGA. The TMS320C6455 DSP and the Xilinx Virtex-5 LX110 FPGA provide the digital signal processing capabilities required by the DVB-T2 standard as well as by further modern communication standards like IEEE 802.11n. Following this hybrid concept of a software/hardware solution has major implementation advantages. While FPGAs are ideally suited for massive parallel processing, DSPs are superior in the implementation of scheduling tasks. By combining both techniques, the proposed system architecture exhibits both advantages. The DSP is the heart of the prototyping platform, controlling and reconfiguring all further hardware components. The Virtex-5 LX110 FPGA acts as a necessary and flexibly adjustable hardware accelerator, providing, e.g., real-time error control decoding capabilities. The DSP is programmed in C++ language using the Code Composer Studio, and all FPGAs are programmed in Verilog HDL (Hardware Description Language) using the Xilinx ISE development suite. To facilitate a high-speed interconnection between DSP and Virtex-5 LX110 FPGA, the authors developed a point-to-point variant, i.e. a simplified version, of the well-known PCI (Peripheral Component Interconnect) bus, allowing a maximum transmission rate of approximately $700\,\mathrm{Mbit/s}$. For the implementation of the DVB-T2 receiver, the error control decoded bit stream is the output of the prototyping platform developed by the authors. To facilitate a low-cost and at the same time standardized interface, the authors rely on a USB 2.0 connection with a maximum achievable data rate of about $400\,\mathrm{Mbit/s}$.

After describing the concept of the underlying reconfigurable prototyping platform, within this section some implementation aspects are emphasized, focusing on the implementation of the DVB-T2 receiver. The received RF signal, prevailing either in the VHF or the UHF band, is first processed by a Thomson DTT73200 digital terrestrial tuner, generating an IF (Intermediate Frequency) receive signal at its output. To circumvent the impact of intermodulation distortions (IMD) caused by I/Q imbalancing, the authors deploy a single heterodyne analog receiver which feeds an Analog Devices AD6655 analog-to-digital converter (ADC) with a maximum sampling rate of $150\,\mathrm{MSamples/s}$. Within the AD6655, the IF received signal is sampled and digitally down-converted. This conversion scheme shows a superior robustness against analog impairments as shown in [9] especially compared to homodyne conversion. Nevertheless, in the proposed fully modular concept, the RF module can be easily replaced by a homodyne solution if necessary. The digitized received signal output by the AD6655 is decimated, digitally down-converted and low-pass filtered before being transferred to the DSP. The digital down-conversion step allows a very efficient implementation of an automatic frequency error correction (AFC) since the integrated NCO (Numerically-Controlled Oscillator) can be reconfigured very easily. Frequency offsets result from impairments in the analog signal processing branches, in particular in deviations of the local oscillator frequencies from the reference value. The Xilinx Spartan-3 FPGA acts as an interface between the parallel data output of the ADC and TIs External Memory Interface which is used to transfer the digital complex baseband signal to the TMS320C6455 DSP for synchronization and demodulation. In order to reduce the load of the digital signal processor, the data transfer between Spartan-3 FPGA and DSP is carried out by using DMA (Direct Memory Access) which allows data transfers without DSP intervention. The petri-net based scheduling of the signal processing carried out on the DSP is depicted in Figure 3. After frame synchronization, a synchronization tracking is carried out for compensating for potentially occurred synchronization mismatches. The synchronization in DVB-T2 is based on the P1 preamble. The subsequent symbol, the P2 preamble, contains signaling information required for the demodulation of the following data symbols. The channel estimation and equalization is based on pilot subcarriers and is processed in frequency domain, followed by the computation of the log-likelihood ratios (LLRs).

The LLRs are then transferred to the Xilinx Virtex-5 LX110 FPGA for LDPC decoding. Again, DMA is used to reduce the DSPs load. Finally, the error control decoded bit stream is transferred to a standard host PC (Personal Computer) via USB 2.0 carrying out the source decoding and the video displaying via an HDMI (High Definition Multimedia Interface)

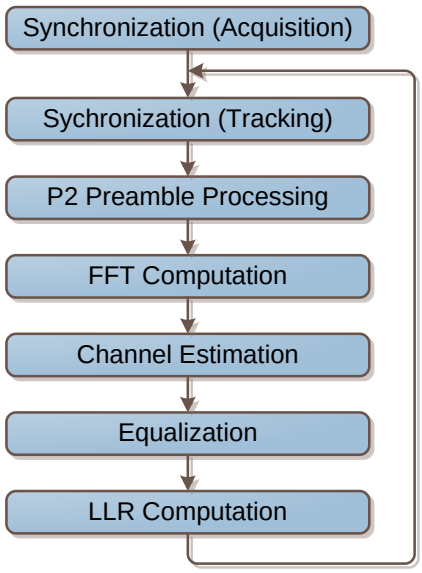

Fig. 3. Petri-net based DSP scheduling

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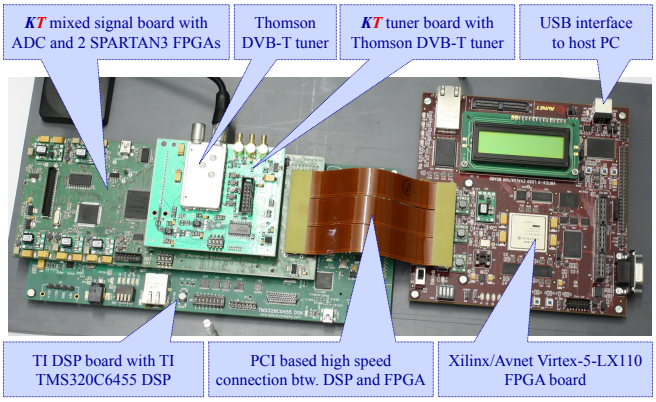

Fig. 4. Photograph of the implemented SDR based DVB-T2 receiver

connection to a full HD display.

III. Reconfigurable Prototyping Platform Implementation

Figure 4 shows a photograph of the reconfigurable prototyping platform developed by the authors, customized for the reception and demodulation of DVB-T2 signals. On the left-hand side of the photograph, a compound of three stacked printed circuit boards (PCB) can be seen. The top is the RF tuner board developed by the authors. This RF tuner board hosts the aforementioned Thomson DTT73200 digital terrestrial tuner. The RF tuner board is connected to the mixed-signal board also realized by the authors. As described before, this mixed-signal board hosts two Xilinx Spartan-3 FPGAs of which one is required for the DVB-T2 receiver. The mixed-signal board is connected to the Texas Instruments DSP board which contains the TMS320C6455 DSP. On the right-hand side of the photograph shown in Figure 4, the Virtex-5 LX110 FPGA evaluation module is located. The interconnection of the FPGA board and the mixed-signal board is a proprietary PCI solution.

IV. Performance

The resulting constellation diagram for the most challenging DVB-T2 mode with an OFDM size of 32768 points and 256-QAM subcarrier modulation is shown in Figure 5. Due to analog impairments such as local oscillator frequency and sampling clock offsets, the degradation becomes higher for increasing QAM symbol magnitudes. Nevertheless, the powerful forward error correction scheme is able to correct the occurring errors. Figure 6 depicts the obtained error performance of the demonstrator in the case of a transmission via a single path channel with additive white Gaussian noise (AWGN), assuming LDPC coding with a code rate of 3/5, a code word length of 64800 bits, 32k FFT and 256-QAM modulated data symbols transmitted over each subcarrier. This error performance was measured for benchmarking. In Figure 6, both the bit error ratio (BER) P_{bit} as well as the block error ratio (BLER) P_{block} are shown versus the signal-to-noise ratio (SNR) $10\log_{10}(E_{\mathrm{s}}/N_0)$. Both P_{bit} and P_{block} are determined at the output of the BCH decoder which follows the LDPC decoder. The LDPC decoding results was determined after a maximum of fifty decoding iterations. Both LDPC and BCH decoders are soft-input decoders. It is found that a P_{block} of 10^{-3} requires an SNR $10\log_{10}(E_{\mathrm{s}}/N_0)$ of less than $16.7\,\mathrm{dB}$. The corresponding BER is approximately 10^{-7} at the same SNR. Furthermore, it was found that the analog single heterodyne receiver allows a superb error vector magnitude (EVM) of less than $2\,\%$. The frequency offset of the RF tuner is lower than $6\,\mathrm{kHz}$ without correction, corresponding to 21.5 subcarriers. This frequency offset can be easily corrected by an automatic frequency correction (AFC) and synchronization algorithm developed and implemented by the authors. The implemented SDR based DVB-T2 receiver was tested using an RF signal which was generated and transmitted through a Rohde & Schwarz AFQ / SMIQ06 combination. The test signal was based on a 256-QAM/32k FFT variant of the DVB-T2 signal. It contained a multiplexed version of three HDTV test video streams provided by the BBC. The gross information rate was $45\,\mathrm{Mbit/s}$. The signal which is generated for the performance analysis is fed into the demonstrator and processed. The resulting bitstream is sent to a PC where the block error ratio is measured. Since the transmitter consists of calibrated measurement equipment, the power level at the antenna input can be controlled arbitrarily. Hence, the sensitivity of the demonstrator can be measured easily. In addition, the demonstrator can be put in a transparent mode which allows to measure the modulation accuracy by calculating the error vector magnitude.

Furthermore, the modular concept of the prototyping platform allows for easily implementing other communication systems beside DVB-T2. Due to the nature of the deployed hardware, the functionality can be changed to support totally

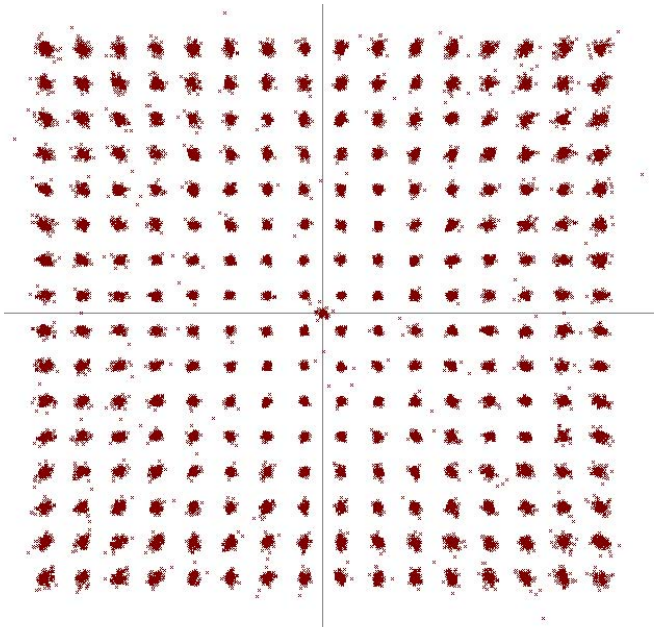

Fig. 5. Constellation diagram of a received and equalized 256-QAM signal

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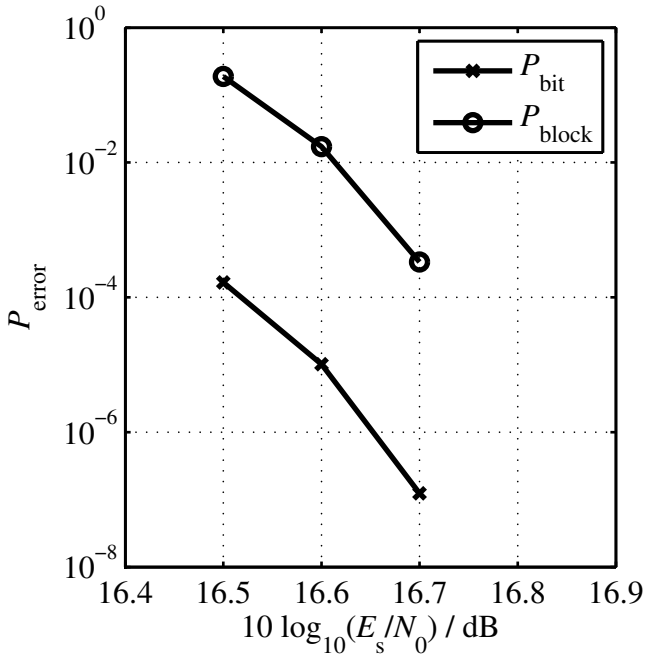

Fig. 6. Error performance

different communication standards by changing the firmware. The clock generation and distribution circuits are software controllable and can match the specification of a majority of the commercially deployed communication standards. The RF down-conversion stage is limited in the support of carrier frequencies and baseband bandwidths, but can be exchanged easily due to the modular concept.

V. Conclusion

Within this manuscript, the authors presented a system concept and setup of a reconfigurable prototyping platform using the example of DVB-T2. This platform combines the digital processing power of high-performance Texas Instruments TMS320C6455 DSP and Xilinx Virtex-5 LX110 FPGA with a single heterodyne analog receiver concept. With this system concept the authors will ease the way towards commercial and highly integrated implementations of communication systems. In addition, the presented platform is ideally suited for research and development for future wireless communication systems.

VI. Acknowledgment

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