Step-by-Step Design and EM Modeling of a 3D Solenoid-based 4 GHz Band-pass Filter (BPF) using Through Silicon Vias

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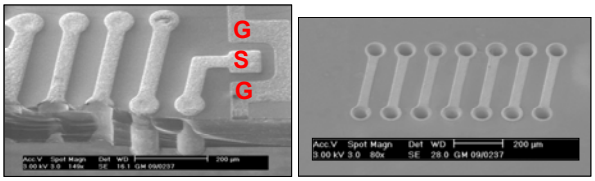
***Abstract*—In this paper, the design of an original fully integrated band-pass filter at 4 GHz using low-aspect ratio Through Silicon Vias (TSVs) is presented. Response of the filter has been simulated within a single BGA (Ball-Grid Array) package implemented on a Rogers substrate. Simulations have been performed with the help of a FEM (Finite Element Method) 3D EM (Electro-Magnetic) simulator. Prior to filter implementation, a comparison between simulated and measured data is proposed on both 3D solenoids and the package in order to calibrate the simulator and validate the simulation methodology. The obtained simulation results are successfully correlated to measurement results. Then the filter is built taking into account the previously defined building blocks (solenoids + packaging) and optimized by taking into account its global environment. The proposed solution allows a clear reduction of the filter footprint compared to discrete devices based implementation. The total area of the filter is 3.6 mm x 2.4 mm. The insertion loss and return loss at 4 GHz are about 2.6 dB and 16 dB respectively.**

Keywords - Finite Element Method, Through Silicon Via, passive integration, filtering, EM simulations.

I. INTRODUCTION

The concept of 3D packaging using TSV stacking is one of the most promising technologies. It can extend Moore's law by stacking and shortening the connection path between memory and logic [1]. Due to the increase in functional integration requirements, more and more assembly house and wafer foundries are looking into 3D TSV technology, which allows stacking of Large Scale Circuits (LSI's) thereby enabling products to be made smaller with more functionality. 3D technology realizes miniaturization up to 300-400% compared to the conventional packaging [2]. Furthermore TSVs are also relevant to develop "more than Moore" applications [3], where passive functions originally lying on the PCB (Printed Circuit Board) can be designed with the help of TSVs using original component architectures such as embedded solenoids (see Fig. 1). In that sense, distributed L, C filters based on TSVs can be investigated and implemented within interconnect dies.

Indeed, the increasing demand of the wireless communications applications requires the radio frequency (RF) receiver to be operated in multiple frequency bands so that users can access different services with a single handset. In designing the RF receivers, a band pass filter (BPF) is added to perform the filtering of unwanted signals and to pass the signal of the specific frequency from the antenna. Filters are either integrated on chip (using planar coils and Metal-Oxide-Metal (MOM) capacitors) or integrated in a hybrid application such as MCM (Multi-Chip Module) lying on a ceramic or organic substrate using a micro strip architecture.



(a) (b)

Figure 1. SEM pictures Top view (a) and bottom view (b) of the 3D solenoïds within GSG (Ground Signal Ground) pads – source IPDiA

Some well known structures have been already successfully implemented and reported [4]. For the former ones, they can suffer from their low quality factors (mainly due to the resistive losses within the planar coils) while the latter ones exhibit high performances but can deviate a lot from nominal behavior compared to silicon due to process spread. An other alternative also consists in implementing the filters on top of the carrier substrate (Printed Circuit Board for example) with the help of Surface Mounted Devices (SMDs). The main advantage of such approach is the high quality factor value that can be reached, but generally they have limited performances at higher frequencies, the total footprint is bigger and the lack of accurate and scalable electrical models limits their applications and implementation in view of a high selectivity of the signals.

In case of fully integrated filters within silicon IC processes, some passive integration dedicated processes have

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been already developed to tackle the low quality factor of the unit components. Devices are generally deposited on HRS (High Resistive Substrate) that clearly limits the effects of eddy currents [3]. Thick top metals are also implemented and copper is often used to reduce the resistive losses. Thickness up to 8 um can be considered in certain cases. Recent achievements have highlighted really good performances for band-pass filter for TV on Mobile applications [5]. For this application, coils exhibit regular planar shape, which provides a good compromise for designers between ease of layout and manufacturing and the electrical performances. On the other side, together with the emergence of new type of interconnects such as TSVs, embedded solenoid implementation within silicon or glass substrate [6] is now considered to easily build a coil-type structure. Several proposals have been done in that sense leading to very promising results [7][8]. In fact, integrated solenoids can be used to produce larger quality factor than in RF BiCMOS/CMOS planar technologies within a given footprint [9]. This increase in quality factor can be attributed to both metal thickness and the specific solenoid property of storing energy according to:

$$Q = \omega \cdot \frac{energy\ stored}{average\ power\ dissipated} \qquad (1)$$

So, in this paper, we propose to take advantage of TSVs implemented with thick patterned metals within an IPD (Integrated Passive Devices) process to design a band-pass filter at 4 GHz. The paper will be organized as follows: Integrated solenoid as well as MOM capacitance will be introduced in the first part; their performances will be presented from an electrical point of view together with their relative precision taking into account the process spread. Solenoid performances obtained from wide-band frequency 2-ports S-parameters measurements will be presented. EM (Electro Magnetic) modeling done with the help of a 3D FEM solver will be also described and compared to measurements.

As the effect of packaging plays a significant role on the device performances, the second part of this study will be devoted to the characterization of a conventional QFN package using a very single test-case. Measurement data will be then used to calibrate the EM simulator.

In the third part of this paper, we report the design methodology and the simulation results for a 4 GHz band-pass Chebyshev filter done using TSVs.

II. 3D INTEGRATED SOLENOIDS

A. Solenoid geometry description

We have already reported the fact that 3D TSV based solenoid can be implemented within a silicon die [9]. This process has been developed by IPDiA (formally NXP semiconductors). Our 3D solenoid uses the thickness of the silicon as the third dimension. Indeed each turn of our solenoid is fabricated with the TSV as the vertical sides. A front side and back side metallization of the bulk wafer leads to connect the top and the bottom tracks, thanks to the TSV, allowing creating loops embedded within the silicon. Thereby we obtain a square section 3D solenoid architecture. On the top side of the silicon, a second level of metal is also used to realize MOM capacitors with a density of 100 pF/mm^2.

Copper is deposited onto front and back sides of a 300 µm depth high resistivity silicon substrate (HRS) according to a pattern defined in Fig. 2. The vias are partially filled with the same metal on the external sides as highlighted by the SEM (Scanning Electron Microscopy) picture in Fig. 1b. Consequently N-turns 3D solenoids consist of N elementary spirals placed side by side and connected in the direction of the pitch between two consecutive vias. Due to the TSV technology process, parameters such as via diameter and via height are fixed and so can not be modified. In our case, the aspect ratio AR (height/diameter) is equal to 4. To avoid mechanical stress, the pitch between two vias is set to a minimum value equal to 125 µm. Nevertheless the dimension of the metal tracks in front and back sides can be modified in order to improve the intrinsic component electrical characteristics as suggested by [10]. Hence the solenoid is defined according to its number of turns N, its width Dy and the metal track width W (that can be different between top and bottom traces). A change in the metal tracks width will also impact the spacing SP between two consecutive metal tracks.

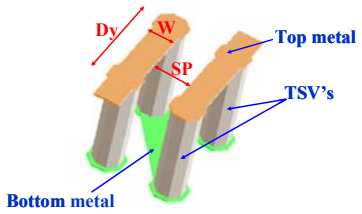

Figure 2. Synoptic representation of 2 turns 3D solenoid (silicon bulk is not represented on this picture)

B. Solenoid measurements

To support our theoretical investigations, solenoids with 1 to 5 turns were designed and grown on silicon. Then the designed test-case inductors have been placed within conventional GSG pads (Fig. 3) and measured using a network analyzer PNA8364B from Agilent Technologies, with high frequency micro-probes. Full two ports S-parameters were performed for each device up to 20 GHz. During the RF characterization, the wafer was stacked to a grounded chuck to ensure a global reference ground to the wafer, the network analyzer and the micro-probes. If no precautions are taken, a short circuit appears between the grounded chuck and the bottom metal tracks of the wafer. As a consequence, a sheet of glass fiber (~100 µm thick, εr = 4.5) has been placed between them. For each measured devices, self-inductance value and quality factor have been extracted on five crystals. In [9], we have already shown that the self-inductance variation versus the number of turns N was really close to a linear law, suggesting a very low inductive coupling between the loops. This is due to the

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minimum pitch defined by the process that is relatively large (=125 µm). As a consequence, the capacitive coupling is also reduced, which allows using the inductors at several GHz. Furthermore, due to the typical geometry of the solenoid, the quality factor is improved up to several GHz compared to classical planar IC coils either in CMOS or BiCMOS processes. A physical lumped elements electrical model was proposed also in [9] to simulate the device behavior versus frequency. This model is indeed really helpful to generate contour plots in order to pick-up the right solenoid parameters (N, W, Dy, SP) and thus decrease the design iterations. By the way, as any other compact model, it is not correlated to the global environment of the device (parasitic coupling, ground rails …). So in view of designing passive filters, we have developed an EM (Electro Magnetic) based model.

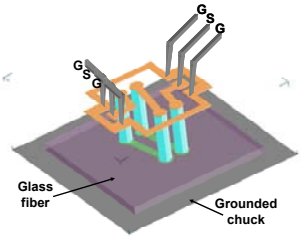

Figure 3. Illustration of the measurement test-bench used to guarantee a good ground reference together with an isolation between bottom metal traces and the chuck

C. 3D solenoid modeling

Dedicated test-cases presented in the previous paragraph have been simulated using the 3D FEM solver EMPro from Agilent. First, TSVs have been defined within the substrate stack taking into account the partial fill of the vias with copper, the barrier between the copper and the silicon bulk (to avoid copper diffusion in the silicon). Geometry of the vias is also simplified: the circular shape of the TSVs is converted to an octagonal one, in order to speed-up the mesh and thus the simulation time without losing any accuracy on the results. Bulk silicon has been described with the help of its relative dielectric permittivity (εr=11.9) and its resistivity - equal to 1000 Ω.cm. A comparison between both self-inductance value and quality factor against frequency is presented in Fig. 4. Self-inductance and quality factor values have been extracted according to the following relations:

$$L = \frac{imag\left(\frac{1}{Y_{11}}\right)}{2\pi \times freq} \quad (2)$$

$$Q = -\frac{imag\left(Y_{11}\right)}{real\left(Y_{11}\right)} \quad (3)$$

Where freq is the working frequency.

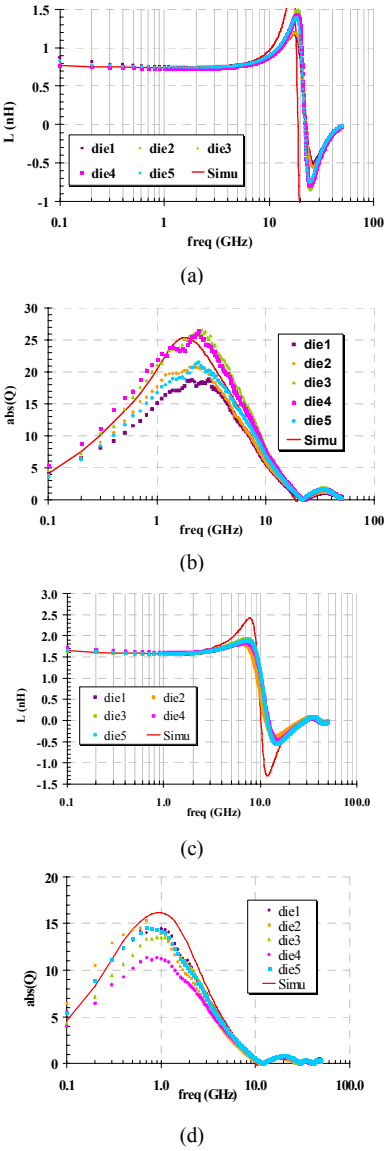

Figure 4. Comparison between measured and simulated data for 1-turn solenoïd (a): self inductance value (b) quality factor and 2-turns solenoid (c): self-inductance value (d) quality factor

From the available test-cases, a pretty good agreement is found for the self-inductance as well as the quality factor variations versus frequency. The SRF (Self-Resonant-Frequency) is also well predicted suggesting that the parallel capacitances are also well evaluated with the proposed approach. Typically, a difference of 3 % is observed on the self-inductance value and 10% on the overall variations of the quality factor. This validates our approach that will be used to design a 3D solenoid based passive filter. By the way, these measurements and simulations have been performed on-wafer without any coating on top of the substrate. In the following part of this paper, we propose to study a single test-case combining a chip, a package and a line on a board to validate our EM tool for packaging applications also.

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III. PACKAGE MEASUREMENTS AND MODELING

Indeed, the emerging applications of wireless communications require effective low-cost approaches to microwave and RF packaging to meet the demand of the commercial marketplace. In that sense, surface mountable packages and especially plastic packages are a cost effective solution for low-cost assembly and packaging. However, plastic packages, whatever their types (standard QFN or flip-chip based solutions such as BGA) contain unavoidable parasitic elements. As a consequence, development of characterization techniques for surface mounted packages is motivated by the need to predict the parasitic behavior of packages at microwave frequencies. In fact, the capability of accurately and easily characterizing packages provides a means to study and correctly model their high frequency behavior. Work in the literature relies mainly on EM simulations [11][12]. In this paper, we will present an "on-wafer" method of measuring the microwave performances of a chain containing a chip, a package and 50 Ω line on Rogers substrate. Final goal of this part is to calibrate the EM simulator (in our case EMPro from Agilent) based on this single test-case.

A. Test-case description and measurement

One of the main problems of package characterization is that the terminals of the lead-frame are not accessible without significant modification to the investigated structure. To overcome the need for this modification, we have divided the test-case into three main parts. A photograph of the test-case is provided on Fig. 5.

So the first part of the test-case is a BiCMOS (NXP in house process) silicon die containing a coplanar line. The line is designed in such a way that it allows GSG probing with conventional micro-probes from Cascade micro-tech. This line is then connected with the help of 4 bond wires (2 for the signal and 2 for each ground path) to the pins of the package. Classical 20 µm diameter gold bond-wires have been considered for this study. Then, to be able to measure the electrical characteristics of the package, it is mounted onto a RO4003C substrate from Rogers Corporation (thickness = 406 µm, εr = 3.38, tan δ = $2.7e^{-3}$). A specific coplanar access is also designed on the substrate allowing also GSG probing (bottom side of the photograph in Fig. 5).

In order to perform 2-ports S-parameters measurements, the package is then opened to access the GSG pads on the chip. Prior to measurements, a SOLT calibration is performed. Four test-cases have been measured up to 50 GHz to ensure a good reproducibility of the measurements. Results are presented in Fig. 6.

The first results clearly show a good reproducibility between the measurements. Insertion and Return loss of the total chain are respectively equal to -1.3 and -10 dB at 4 GHz, which makes such a package suitable for several GHz applications. Of course, many improvements can be considered to improve these performances (ground connection, wire loop profile, down bonds implementation). But, these techniques won't be addressed in this paper.

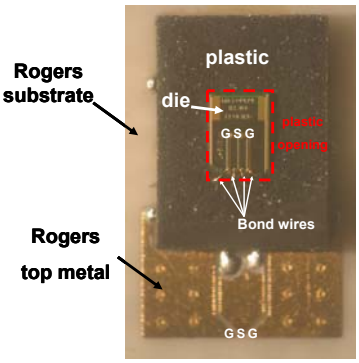
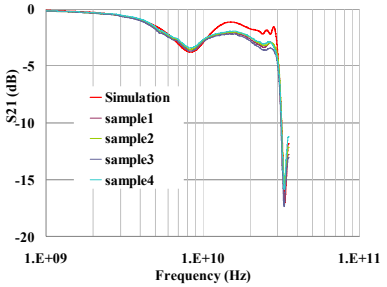
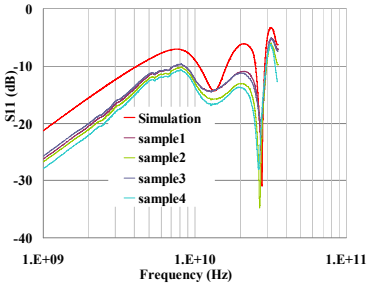


Figure 5. Photograph of the designed test-case suitable for microwave package characterization and modeling



(a)



(b)

Figure 6. Comparison between measurements and simulated data vs. frequency on the package test-case – (a) transmission parameters, (b) reflection parameter

B. Package modeling

The aim of this paragraph is to calibrate the 3D FEM solver EMPro from Agilent to correctly handle the S-parameters variations of the previously measured test-case. The 3D EM model should estimate the electrical performances of the package as accurately as possible, but on the other hand, should not be too complex for the EM simulations of more complex block. The following methodology has been applied:

- Bond wires cross-section have been first described with a square shape. Generally speaking, all round shapes should be avoided as much as possible as they are really time consuming for the simulations and the 3D mesh generation.
- Bond wire profiles were estimated based on a circle shape assumption as proposed by Alimenti and al. [13].

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- Package terminals are defined into two equal steps (each is 100 µm thick) to have accurate modeling of the thick metal. One should try also to approximate their geometries with a few corner points as possible but the modifications should not affect the electrical response of the simulator.
- Coplanar ports have been used on both the chip and substrate lines.
- All dielectrics are defined with finite bricks taking into account their relative permittivity and the loss tangent or the conductivity. Plastic brick is open with an "Air" brick in order to stick as much as possible to the measurement configuration.
- The common ground reference was set to the bottom metal of the Rogers substrate

Both reflection and transmission S-parameters obtained from EM simulations are plotted on Fig. 6 together with measured data. The simulated data corroborates the measured ones with a good accuracy up to several tenth of gigahertz. To conclude this part, the EM simulation tool enables relatively accurate and complex package analysis. So based on these two previously studied test-cases (solenoid and package) the FEM solver is calibrated and ready for embedded filter design with TSVs.

IV. FILTER DESIGN AND MODELING

Based on the previous building blocks that have been studied here before (i.e., package and solenoid measurements together with EM modeling), this part will focus on the design feasibility of a 4GHz band-pass filter. Objective is to design a band pass filter with a maximum of 4dB insertion loss.

A. Schematic design

In a first time, a third order Chebyshev architecture has been considered to design the filter prototype. By the way, taking into account coefficient in [14] and applying the well known transform from low-pass to band-pass filter, lead to an inductor value in the serial electrical path that is equal to 9.13 nH. Such an inductor will have a high serial electrical resistance that will seriously affect the insertion loss of the overall filter and will also have a Self-Resonant Frequency to close to operating frequency clearly limiting its usage. So, a choice has been made to split the filter into two different parts as shown on Fig. 7 and already proposed in [5]. The first part is a 5th order low-pass filter while the second one is a 3rd order band-stop filter. Both are Chebyshev filters. By doing this, only MOM capacitors and small inductances values (i.e., 451 pH for L6 and L10) will be present in the serial path of the filters. This approach allows reaching the specified level of insertion loss.

All inductors will be designed with the help of TSVs with the same architecture as the ones presented in the first part of this document. The quality factor of inductors L6/L10 have been simulated prior to implementation and are equal to 10, which is sufficient for the targeted application. For inductors placed on the parallel paths (i.e., L1, L3, L5 and L9) their impact is really low regarding the insertion loss.

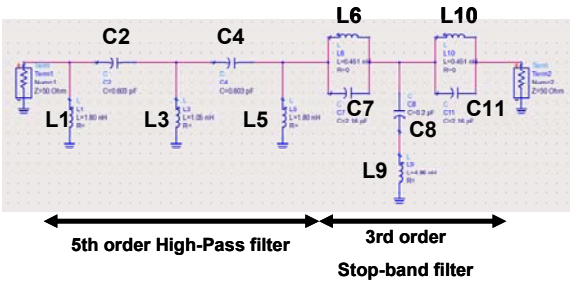

Figure 7. Schematic view of the band-pass filter considered for this study

For the capacitors, a choice has been made to use the "free" MOM capacitor offered by the process. In fact two metallization are present and can be patterned as well on the top-side of the wafer. They are separated by a classical oxide with a density of 0.1 nF/mm^2. A very low serial resistance value induced by the capacitor is expected to results from the use of two thick copper layers as device electrodes. Furthermore, very precise values of capacitance can be obtained since its relative precision is driven by the oxide thickness, which is really low (+/- 5%).

All these components will of course interact one with another leading to a change in the frequency response of the filter. That's why, a top level EM simulation is required to adjust and optimize the topology of the overall filter taking into account the interconnections as well as the ground return path.

B. Layout implementation

Special care has been taken to optimize the electrical resistance on the serial path. Wherever possible, the RF path was designed by stacking both levels of metallization connected together with the help of vias. Orientation and aspect ratio of capacitors have been chosen in such a way to minimize the resistive losses. A view of the simulated filter is shown on Fig. 8.

First order dimensions of the solenoids (Dy, N) have been deduced from the analytical model provided in [9]. The value of the ground path inductance (metal tracks + bumps) is then taken into account as they participate to the self-inductance value from the RF path to the ground (inductors L1, L3, L5 and L9). The metal track inductances have been calculated in reference to partial inductance concept proposed by Ruehli and Zhong [15][16]. Electrical parameters of the bumps have been evaluated by calculation and single EM simulations as proposed in [17].

LC tanks (L6, C7 and L10, C11) in the stop-band filter have been realized with one-turn solenoids. Then prior to top simulations, each solenoid of the filter is placed with care in order to avoid as much as possible coupling between them. Typically the maximum space is considered, and an orientation of 90° between each inductor is applied to minimize magnetic coupling. Dimensions of the whole filter are 3.6x2.4 mm^2 and clearly outperform conventional microwave structures such as hairpin filter for similar application [18]. The full structure is then simulated within

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the package with the bump connection to the Rogers substrate. Results are presented on Fig. 9.

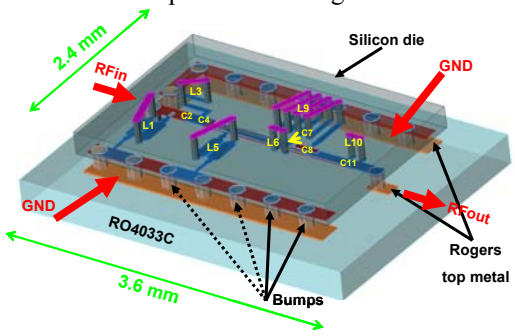

Figure 8. Top view of the simulated band-pass filter. Plastic of the package is not represented on the picture for clarity reason

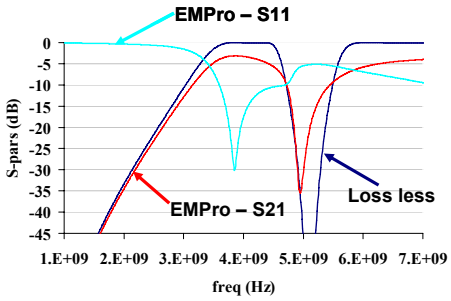

Figure 9. Simulations results of the proposed filter. Dark blue line corresponds to loss-less schematic filter simulated with ADS© schematic

From the available results, the filter exhibits insertion and return loss of 2.6 and 16 dB respectively. Insertion losses are clearly within the specifications even if they are higher than classical micro strip filters. The main contributions to the insertion losses are both inductors L6 and L10 for whom electrical resistance increases very fast with the frequency. This approach gives indeed good results in case of moderate loaded Q (few units) but won't be accurate in case of narrow fractional bandwidth where higher loaded Q-factors are required. For these very specific applications classical micro strip filters deposited on low loss substrates such as ceramic should be considered. TSVs can be used to build compact filtering function up to several GHz.

V. CONCLUSION

This paper reports a novel approach based on TSVs to integrate and miniaturize band pass filter for L and S-band applications. This kind of approach is very interesting for moderate loaded quality filter devices. It can be used within hybrid systems where passive functions are combined with improved interconnections in order to obtain high performance devices. A simulation methodology based on a step by step calibration of the FEM tool and measurements on single 3D structures is described. It allows at the end simulating the filter in its packaging environment. From the simulation results, we have demonstrated the feasibility of TSV based BPF with insertion loss of about 2.6 dB at 4 GHz.

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