A New Front-End Readout Electronics for the ALICE Charged-Particle Veto Detector

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***Abstract*—The A Large Ion Collider Experiment (ALICE) upgrade strategy is based on collecting more than 10 nb^{-1} of Pb-Pb collisions at luminosities of $6x10^{27}$ $cm^{-2}s^{-1}$ which corresponds to a collision rate of 50 kHz for Pb-Pb and 200 kHz for pp and p-Pb. Such high beam luminosity requirements cannot be met with the presently existing electronics having a low readout rate of 5 kHz. This work presents the design of a new front-end readout electronics for the Charged-Particle Veto detector (CPV) module located in PHOton Spectrometer (PHOS). The proposed new architecture, when compared to prior systems, allows the parallel readout and processing of all 480 silicon photomultiplier pads that are connected to digital signal processing cards. Preliminary results demonstrate that this work will enable the CPV detector to reach an interaction rate of at least 50 kHz. The system design consists of three modules, each containing two segment boards, two Readout Common Boards (RCBs) and 16 digital signal processors called DiLogic cards. This paper presents the architecture layout and preliminary performance measurement results for the proposed new design. This work concludes with recommendations for other future planned updates in hardware schema.**

Keywords*— *Electronics; Detector; Field-Programmable Gate Arrays; CPV; ALICE; PHOS.

I. INTRODUCTION

The ALICE experiment is dedicated to study and collect data for comparison about heavy ion and proton-proton collisions in heavy ion-physics. The current system still leaves open physics questions that need to be addressed, and these questions relate to, among others, hadronization, nuclei, long range capability correlations and small x-proton structure [1][2]. The photon spectrometer PHOS is a lead-tungsten calorimeter designed to detect, identify and measure the 4-momenta of photons. The CPV is a charged particle veto detector for photon identification located in PHOS consisting of a multiwire proportional chamber (MWPC) with cathode readout. CPV electronics consist of dedicated Application Specific Integrated Circuit (ASIC) devices in each column, Gassiplex for analogue signal processing and DiLogic for handling the digitized information. Every column consists of 10 Gassiplex cards, called 3-GAS cards interfaced directly on the backside of the MWPC cathode. A customized electronic board called 5-DiLogic contains five channels of 12-bit Analogue-to-Digital Converter (ADC) modules and five DiLogic (5-DiLogic) processors [3]. Each column contains 480 pads connected with two 5-DiLogic cards and a group of Field-Programmable Gate Arrays (FPGAs) called column and segment controllers that are used to process signals from a column and provide the necessary interface with DAQ (Data Acquisition) and Central Trigger Processor (CTP) systems. The CPV consists of three electronic modules, one of them shown in Figure 1, where each CPV module contains sixteen columns and 7680 channels for amplitude analysis.

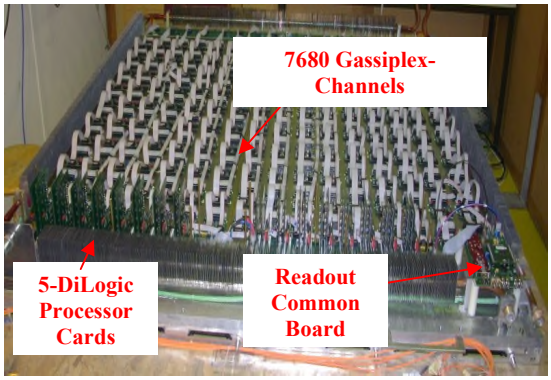

Figure 1. Hardware for one CPV module.

A typical event size consists of 1.3 Kbytes for Pb-Pb particles. The maximum event readout rate that the detector can presently reach is 10 kHz for an occupancy of 1% [4], therefore, due to this technical limitation, a new front-end readout electronic system is being developed to collect more than 10 nb^{-1} of Pb-Pb collisions at luminosities of up to $6x10^{27}$ cm^{-2} s^{-1}.

The rest of the paper is structured as follows. Section 2 gives an overview of the developed system hardware. Section 3 provides a description of the implemented firmware architecture. Preliminary results are shown in Section 4. Finally, Section 5 presents the conclusion and future work.

II. OVERVIEW OF SYSTEM HARDWARE ARCHITECTURE

Figure 2 illustrates the architecture of the new Front-End Electronic (FEE) Readout detector hardware. The proposed hardware architecture for one module includes the re-design of a motherboard interface card called Segment board used to

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concurrently process four DiLogic cards via an FPGA Altera column controller card containing a 28nm Cyclone V GX device. A Readout Common Board (RCB) is used for transmitting information to run the experiment over a radiation tolerant Gigabit transceiver (GBT) link chipset [5] to a Data Acquisition (DAQ) Common Readout Unit (CRU) at a high speed of (~5 Gb/s). The custom RCB card solution uses a Stratix IV FPGA device with four full duplex transceivers to transfer event data from column controllers to the GBT over optical Small Form-factor Pluggable (SFP) link for processing by DAQ CRU. Furthermore, the radiation-hard GBT link provides the simultaneous transmission of trigger and experiment control data over the same optical link. One SFP for Versatile transceiver link (VTRx) to CRU and a Detector Data link version two (DDL2) interface shall be optionally included to comply with ALICE standards. The newly custom developed hardware shown in Figure 2 enables the simultaneous readout of all column analogue patterns concerning the 480 channels thus drastically reducing the readout time of DiLogic cards by more than 50% when compared to the present CPV and High Momentum Particle Identification Detector (HMPID) readout detector systems. Additionally, this architecture shall reduce the implementation costs because, unlike the existing system, every FPGA column controller is processing signals from two columns instead of one.

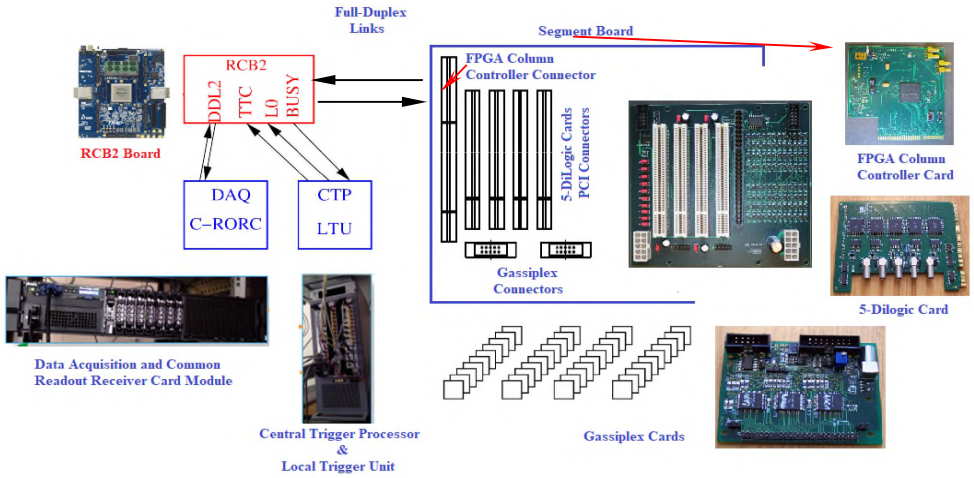

Figure 2. Block diagram of custom developed front-end electronic cards.

III. FIRMWARE DESIGN AND DEVELOPMENT

The firmware is divided into two separate top system VHDL (VHSIC Hardware Description Language) modules for column and RCB or Readout Receiver Card (RORC) controllers.

A. RCB Top System Module

The RCB Top level entity combines all lower level entities, as shown in Figure 3, into the Altera FPGA controller. The GBTx_BANK entity includes several GBT links, where each GBT link is composed of a Gigabit Transmitter (GBTx) component that encodes and scrambles transmitted parallel data, a Gigabit Transmitter/Receiver (GBTRx) component that decodes and descrambles incoming data, and a Multi-Gigabit

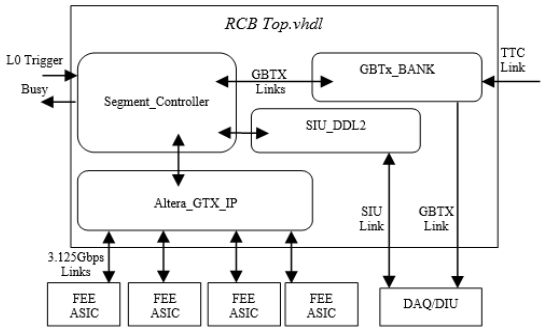

Figure 3. RCB control top VHDL module.

Transceiver (MGT) that serializes, transmits, receives and de-serializes the data. The RCB segment controller VHDL module is responsible for the synchronization logic between the FPGA Transceivers, GBTx link and the Standard Interface Unit (SIU) DDL2 module. Additionally, it processes L0 CTP signal via the Timing, Trigger Control system (TTC) and issues a Busy flag for the reduction of the overall dataflow. The Busy flag is issued from the arrival of the L0 trigger to the end of the transmission of event data, as shown in Figure 6. The RCB segment controller includes also the implementation of the standard SIU protocol as an optional feature for the event data transmission to DAQ or Destination Interface Unit (DIU) experiment recorder.

Figure 4 illustrates the command sequence adopted and implemented in VHDL RCB Top module for transmitting event data from the FEE to RCB or Readout-Receiver Card (RORC). The transmission of the Ready to Receive (RDRYX) command is then acknowledge by SIU and followed by a group of commands, as explained in [6]. The maximum DDL2 data transfer rate between SIU and the DIU is 5.125 Gb/s full Duplex.

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B. Column Controller Top System Module

A VHDL top entity implemented in the Cyclone V GX column controller FPGA device consists of at least two main low-level components called Gassiplex.vhd and Read_sm_simple.vhd. The Gassiplex.vhd component is responsible for the control logic of the Gassiplex chips, consisting of a charge-sense amplifier with a long decay time to acquire the detector analogue signal.

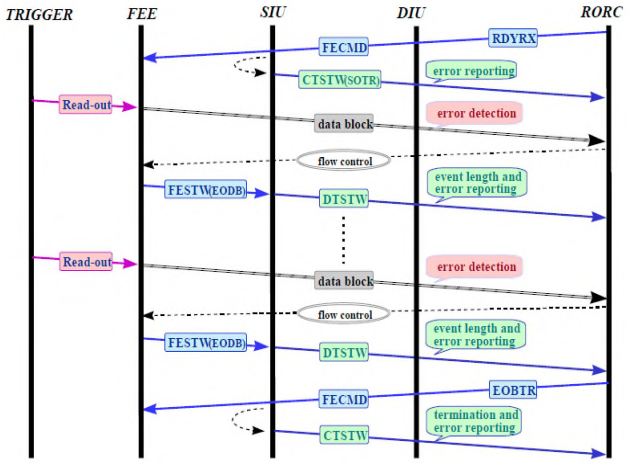

Figure 4. The event data transmission transaction [6].

A Track/Hold (T/H) signal is used to store charges in Gassiplex sampling capacitors using T/H switches. A burst of clock pulses triggered by the column controller FPGA device is then generated to operate the multiplexed readout of the stored charges on a single output line. The Read_sm_simple.vhd contains the hardware logic for the simultaneous readout of two 5-DiLogic cards, as described in [7]. The 10 MHz clock is used for reading DiLogic First-In, First-Out (FIFO) memory. Every 5-DiLogic card contains five DiLogic signal processing chips each having a FIFO of 512 18-bit words, strobe and enable pins StrIn_N, EnIn_N, EnOut_N to initiate and indicate the termination of FIFO readout [8][9]. Each DiLogic chip is put in analogue readout mode when the EnIn_N is set low. Successive StrIn_N cycles cause all DiLogic modules in one 5-DiLogic card to sequentially output the digitised data on an 18-bit data bus starting with the simultaneous readout of the first DiLogic chips labelled DiLogic 0 and DiLogic 5 in the chain, as shown in Figure 5.

An enable signal is then passed from the EnOut_N pin to the EnIn_N pin of the next DiLogic module after finishing the transfer of digitised data for one event-word on the data bus. The concurrent readout of DiLogic cards contributes to a two-fold increase in reading event data from DiLogic cards when compared to the previous and present CPV electronics architecture.

Each event-word contains the selected channel address and digitised amplitude information that need to be transferred via the FPGA transceivers at a rate of 3.125 Gbps then finally to the RCB controller for further formatting and transfer to DAQ.

The RCB and column controller's FPGA transceiver IP blocks include a built-in 8B/10B encoder decoder, byte serializer and deserializer modules enabling the simultaneous transmission of data packets from various FPGA column controllers to always start in a known byte lane and therefore allowing the RCB FPGA controller to correctly decode and properly recover the event frame before any further processing by the RCB fabric. Additionally, on-chip FPGA power supply decoupling to satisfy transient current requirements at high frequencies of 3.125 Gbps have been configured so to reduce the need for on-board decoupling capacitors.

The timing diagram obtained via Altera Signal Tap Logic Analyzer for a data block transfer initiated on receiving L0 trigger signal from CTP for the event-word number 3354h consisting of 10 words (40 bytes) for Common Data Header (CDH) followed by event data from RCB to DAQ is shown in Figure 6.

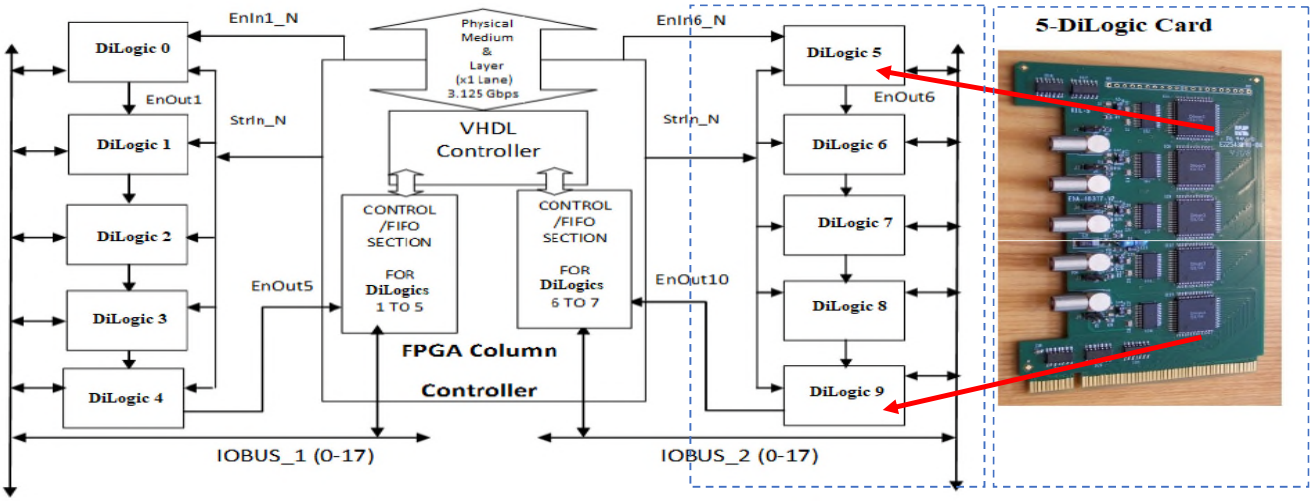

Figure 5. FPGA column controller card for the simultaneous readout of two 5-DiLogic card processors (right) [8].

Figure 6. Timing diagram obtained using Altera signal-tap logic analyser for data transfer between RCB and DAQ.

IV. PRELIMINARY MEASUREMENT RESULTS

A test jig was setup to evaluate the prototype performance of this new readout electronics architecture. The test jig, shown in Figure 7, consists of a Windows workstation terminal for FPGA programming, a Linux terminal for displaying performance results, two RORCs modules and DAQ servers for storing event data, and a Local Trigger Unit (LTU) for issuing the CTP L0 trigger signal. The busy time of the data collection is mainly defined by the CTP waiting time for the completion of the readout electronics to transmit event data from FEE to DAQ server. The detector busy time due to readout in general depends on the event size. Increasing the trigger rate up to 200 Hz, the measured busy time averaged over a one-minute time interval and, as shown in Table I, is 10 us, which is equivalent to an estimated event size of 2.6 Kbytes (2.5 Columns, 5.2% occupancy of total detector channels). This measurement result leading to an estimated event readout rate of 100 kHz is above the required target for a detector occupancy of 1.3 Kbyte Pb-Pb collisions.

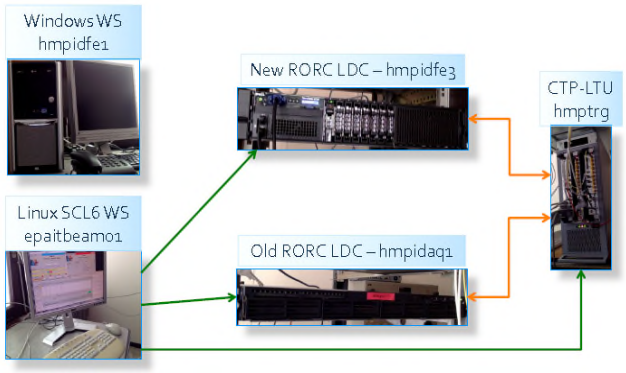

Figure 7. Test jig setup for CPV front-end readout prototype electronics.

The event readout rate measurements of the prior system is shown in Figure 8, thus indicating a maximum estimated readout rate of 5 kHz, twenty-fold slower than this work. The major contribution of our work is the re-design of new electronics, including concurrent readout of DiLogic cards and use of high speed 3.125 Gbps FPGA transceiver links. Another test workbench containing a Cyclone V GT 28 nm FPGA technology was setup in [10] to characterize GBTx performance in Single Event Upset (SEU) and therefore allow GBTx users to estimate SEU errors. GBTx was irradiated using high penetration particles at different angles to estimate the SEU and possible bit-error mechanisms under a luminosity of 10^{34} $cm^{-2}s^{-1}$. The location of the proposed new readout electronics presented in this work will be in the ALICE detector where the measured radiation doses are estimated to be 0.1 kRad and $1.9x10^{10}$ charged particles/cm^2, which puts CPV electronics in a safe operating side by 3 to 4 orders of magnitude [11].

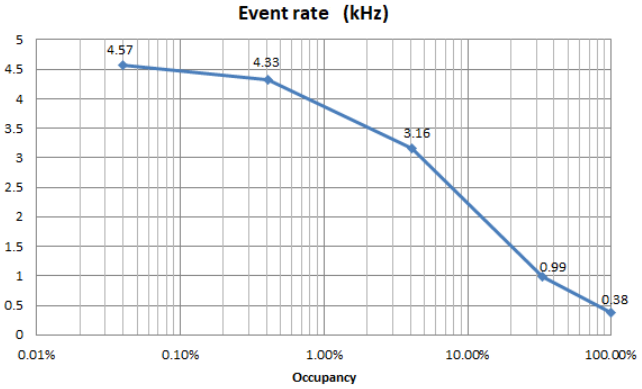

Figure 8. Estimated event readout rate for prior system.

TABLE I. ESTIMATE READOUT RATE FOR VARIOUS EVENT SIZES

Event Size (Bytes)	~Busy Time(us) [This work]	Detector Occupancy (channels)	Number of Columns
536	5.62	0.5 Columns	1%
1196	6.68	1 Column	2.1%
1752	7.56	1.5 Columns	3.125%
2152	8.22	2 Columns	4.1%

Additionally, as described in [12], to detect and protect the system against errors caused by SEU in the FPGA memory cells, a threefold way is to be adopted:

- An efficient error detection scheme based on parity check logic,

-8/10 bits of data coding as part of the DDL2 and GBTx/GBTRx low level protocols have been implemented,

-A Cyclic Redundancy Check (CRC) will be accompanying data on its way between FEE and RCB board.

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The obtained preliminary measurement results shown in Table II indicate an event readout time of ~10 us (100 kHz) for this new architecture leading to a performance improvement in data transfer rate between column controllers and DAQ by almost a factor of two when compared with the present Scalable Readout Unit (SRU) (~21us), Time Projection Chamber (TPC), 100us for High Momentum Particle Identification (HMPID) readout detector electronics as reported in [13], [14] and [15] respectively.

TABLE II . READOUT RATE COMPARISON WITH OTHER DETECTORS.

Detector	**Estimated Readout Rate (us)**
(this work)	10
SRU [13]	21
TPC [14]	33
HMPID [15]	100

V. CONCLUSION

This paper presented the design of a new CPV Front-end Readout electronics system which attains the ALICE Readout rate goal of 50 kHz. The preliminary prototype measurements indicate an estimated event Readout rate of 100 kHz, twice the target value. The newly designed upgrade offers significantly improved electronics performance. Such an improvement in event readout rate when compared with the prior CPV, TPC, HMPID and SRU readout detector electronics is mainly due to the parallel readout and processing of column controllers and the adopted GBTx/SIU transceiver link speeds between DAQ and readout electronics of around 3.125- 5Gb/s. Additionally, the integrated CRC hard Intellectual Property (IP) FPGA block, shall detect and correct errors due to SEU, thus ensuring a reliable operation of the newly developed CPV electronics. A further study to be considered is the evaluation of data reliability versus the improvement in readout trigger rates.

Initial prototype cards have been completed and full production of all electronic cards is planned to be ready in the second half of year 2018. Finally, the old 700 nm 5-DiLogic card technology shall be replaced with an ASIC chip, thus leading to a better system performance, throughput and maintainability.

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