A Low-Power Passive Mixer Receiver for Software Defined Radio (SDR) Applications

Pierre Bousseaud, Emil Novakov and Jean-Michel Fournier
Institut de Microélectronique, Electromagnétisme et Photonique (IMEP-LAHC),
MINATEC – 3 parvis Louis Néel, B.P. 257, 38016 Grenoble, France
e-mail: pierre.bousseaud@minatec.grenoble-inp.fr, novakov@minatec.grenoble-inp.fr, fournier@minatec.grenoble-inp.fr

***Abstract*— Software Defined Radio (SDR) is a promising concept for the next generation of low-power portable wireless devices. Different communication standards can be processed just by changing the software in the transmitter. This approach allows great flexibility as well as hardware cost reduction. In this paper, we describe discrete-time passive mixer architecture for Radio Frequency (RF) direct sampling receivers. This architecture can achieve wideband quadrature demodulation and is suitable for SDR applications. The performances of the architecture are evaluated by simulation. Currently, we are working on the design of an Integrated Circuit (IC) that will implement a quadrature sampled I/Q receiver front-end. The IC is based on a 130nm CMOS technology. The receiver should be able to work in the 868MHz and 2.4GHz ISM bands. The expected power consumption is less than 2 mW.**

Keywords-Software defined radio; RF sampling; discrete-time mixer; linearity; QAM; I/Q; BER; noise figure; filtering; phase noise; blockers.

I. INTRODUCTION

The pervasive wireless applications and the presence of multiple communication standards based on different modulations, with variable channel bandwidth and carrier frequencies have motivated the development of multi-band and multi-standard radio communication technologies like the Software Defined Radio (SDR). On the other hand the CMOS technology's scaling allows now the fabrication of fully integrated radio transceiver chips able to work practically in any available frequency bands [1]. The final goal of the SDR is to receive a plurality of standards on just one single chip, whose functionalities can be updated by software only. The ideal SDR receiver hardware is composed of an antenna immediately followed by an Analog-to-Digital Converter (ADC) followed by the digital signal processing unit. Nevertheless, sampling a 2.4 GHz Radio Frequency (RF) signal at 4.8 Gsample/sec and 12 bit amplitude resolution would consume too much power which makes such approaches clearly unrealistic for miniaturized battery powered devices. In a more practical approach the ADC can be located at the Intermediate Frequency (IF) output of a frequency mixer (down-converter) in a standard super heterodyne RF receiver. Another possible solution is to use direct RF sampling mixer to down convert the wanted RF frequency band around the DC component and to amplify and process the band-pass signal at low frequency.

By using N paths sampling structures it is possible to sample the RF signal on N passive elements such as switched capacitors with both filtering and down-conversion at base-band [2]. This permits to greatly reduce the constraints for the ADC. Some receivers based on this principle have already been studied, implemented and tested by different research groups [3], [4], [5]. They show very interesting properties concerning the linearity and the power consumption. It is interesting to note that with such structures, very high Q pass-band filters can be realized at high frequency [4]. They easily replace RF SAW filters or LC structures which are bulky, costly and difficult to integrate.

The goal of our project is to design, simulate, implement and evaluate passive four paths mixer architecture for direct RF sampled conversion. In this paper we present the receiver architecture as well as the simulation results of its performances. The sampled receiver is designed to work with Quadrature Amplitude Modulated (QAM) signals but can also work with Amplitude Modulated (AM), Frequency Modulated (FM) and Phase Modulated (FM) signals. The complete receiver front-end will be further fabricated in a 130 nm CMOS RF technology.

Section II presents the RF sampling mixer structure and its basic parameters. Section III presents Matlab simulations of the receiver [6]. Section IV defines the implementation characteristics of the receiver and final conclusions are drawn in Section V. This paper is an intermediate report of a "work in progress".

II. FOUR PATHS MIXER ARCHITECTURE

A. Conventional and 4- paths structure

The conventional I/Q passive mixer structure is shown in Fig. 1. For a QAM modulated RF signal $V_{RF}(t) = A\cos(\omega_0 t+\varphi)$ where w_0 and φ are respectively the carrier pulsation and phase. During the symbol period A and φ are constant. In the passive sampling mixer, I and Q are obtained on two different sample/hold circuits by separating their sampling instant by $T_0/4$, where T_0 is the signal's period ($T_0 = 2\pi/\omega_0$). At the sampling time $t_0 = 0$, $I(t_0) = A\cos[\varphi]$. At the sampling time $t_1 = t_0 + T_0/4$, $Q(t_1) = A\cos(\varphi + \pi/2) = -A\sin(\varphi)$. In this way it is possible to find the magnitude A and phase φ of the RF signal in an orthogonal basis I/Q created by the voltage values sampled at the moment t_0 and t_1 as follows: $A = (I^2+Q^2)^{0.5}$ and φ = -

 ISBN: 978-1-61208-193-9

arctan(Q/I). Nevertheless, in such architecture due to the low conversion gain the noise figure is high, thus severely limiting the high frequency performances.

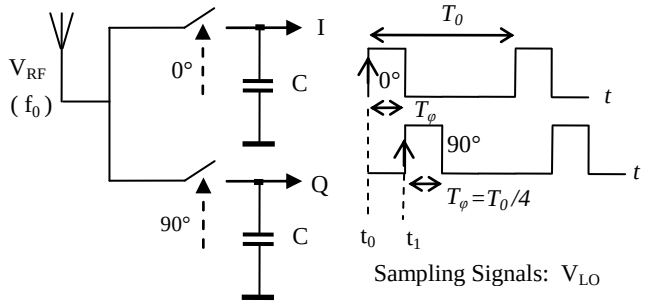

Figure 1. Classical I/Q sampling mixer

It is possible to improve the two phases I/Q sampling mixer by sampling the RF signal at four different points. The four phases mixer operation is based on the relationships: $Acos(\varphi + \pi) = - Acos(\varphi)$ and $Asin(\varphi + \pi) = - Asin(\varphi)$. The structure of the mixer is shown in Fig. 2. Now, *I* and *Q* redundant information are obtained by sampling data *I*+ and *I*- during phases 0° and 180° at and data *Q*+ and *Q*- during phases 90° and 270° respectively. If we subtract both *I*+ and *I*- as well as *Q*+ and *Q*- we'll have $I = I^+ - (I-) = 2Acos(\varphi)$ and $Q = Q^+ - (Q-) = 2Asin(\varphi)$. The power gain is improved by 6 dB and in the same time the Noise Factor (NF) is reduced by 3 dB for each *I* and *Q* paths.

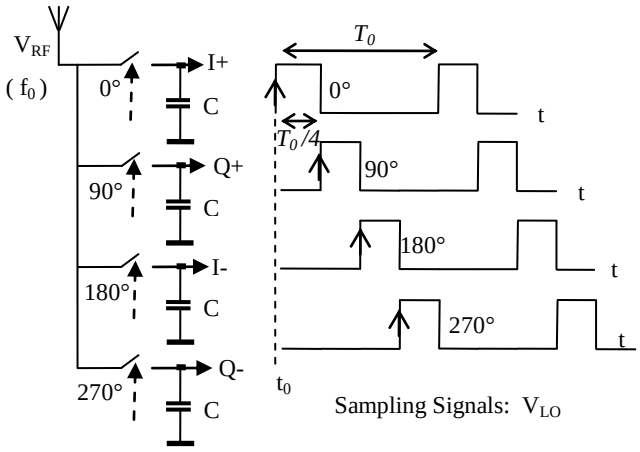

Figure 2. Passive four paths mixer (left) and clock scheme (right)

Further improvement can be obtained by using a fully differential topology. In this case, as shown in Fig. 3, the differential RF signal is sampled on eight different paths and the corresponding values are stored in two capacitors. The differential RF signal can be generated by either a transformer or a single-to-differential buffer amplifier before the sampler. This system is able to work without Low Noise Amplifier (LNA). The gain stage (G) can be moved to the base band signals *I* and *Q* thus increasing the noise figure of the receiver. This sampling scheme has multiple advantages. It is possible to reduce significantly the even order harmonic terms created by the non-linearity in the transistor forming the switch.

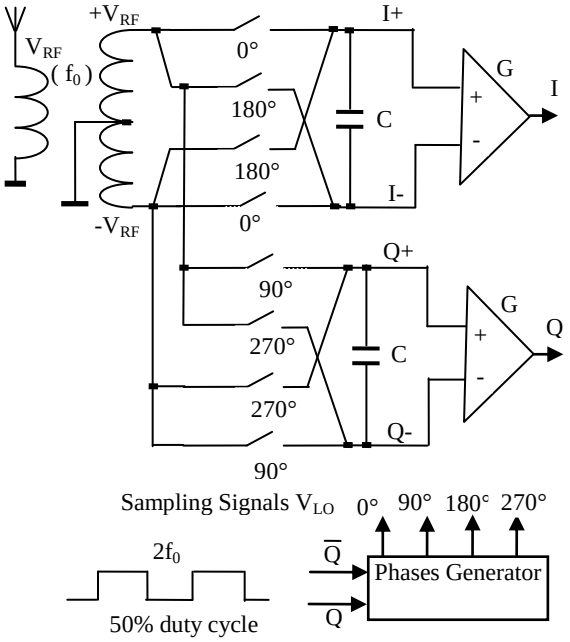

Figure 3. Differential sampling mixer and phase generator

At the sampling moment two opposite switches are activated at the same time. This allows the compensation of the charge injection phenomenon in the switch which causes a distortion in the amplitude of the sampled RF signal. Finally, the error caused by the clock feedthrough is completely rejected [6]. Indeed this error signals appears as a common mode voltage on both top and bottom plate of the capacitor *C*. At least 20 dB of improvement can be done concerning the IIP2.

B. Conversion Gain and Filtering

When the received signal V_{RF} and the sampling signal V_{LO} in Fig. 2 have the same frequency, the difference of frequency seen by each capacitor *C* is null and their equivalent impedance is infinite. Each capacitor behaves as an open circuit. In this case the mixer detects the complex envelope of the modulated signal V_{RF} without attenuation. If *D* is the duty cycle of V_{LO} ($D = T_\varphi / T_0$) the conversion gain (*CG*) of the sampler at the carrier frequency f_0 is given by:

$$CG = \sin c(D) \qquad (1)$$

When the two signals V_{RF} and V_{LO} are with different frequencies each capacitor observes a periodic sliding of V_{RF}. The equivalent impedance is now non infinite. C starts to conduct and provides some voltage attenuation. If we consider one branch of the mixer, a first order low-pass filter if formed by the antenna resistance R_a, the conducting switch resistance R_{on} and the capacitor *C*. By choosing a time constant $\tau = (R_a + R_{on})C$ higher than the period of the

modulated signal we can filter the input signal V_{RF}. If $f_{IF} = f_0 - f_{LO}$ is the difference of the frequency between the radio signal and the sampling signal and $f_C = 1/(2\pi\tau)$ is the cut-off frequency of the low-pass filter, the transfer function of the sampler at the base-band is given by [3]:

$$H(f_{IF}) = \frac{\sin c(D)}{1 + j\frac{f_{IF}}{Df_C}} \quad (2)$$

The equivalent bandwidth B of the sampler is:

$$B = \frac{D}{2\pi(R_a + R_{on})C} \quad (3)$$

The system is equivalent to a frequency converter and a band-pass filter at the same time. By changing the V_{LO} frequency it is possible to down convert V_{RF} and by choosing the duty-cycle it is possible to control the bandwidth of the converted signal.

C. Harmonics rejection

The sampling receiver architecture is based on the N paths filtering concept [2]. At the base band the sampler down converts the signals V_{RF} with harmonic frequencies multiple of f_{LO}. By combining signals from the different paths some harmonics can be suppressed. Using a N paths mixer, only the harmonics of the form $(Ni+1)f_{FLO}$ remain (i=±1, ±2, ±3 …). For the four path mixer in Fig. 3 (N=4) the harmonics (-5, -4, -2, -1, 2, 3, 4, 7 …)f_{LO} are rejected.

D. Noise

In the mixer there are two main noise sources: the thermal noise of the antenna and the thermal noise of the switch resistance R_{on} when the switch it turned *on*. The major contributor to the noise is the resistance of the switch. That's why this resistance must be as low as possible. That imposes the use of larger transistors with higher Wide to Length (W/L) gate ratio. This also increases the parasitic capacitor between the gate and the source, which leads to degradation of the linearity due to more charge injection phenomenon [5]. That's why a trade-off must be found between linearity, noise factor and sizing of transistors realizing the switches. The Noise Figure (*NF*) of the system is given by [4]:

$$NF = (1 + \frac{R_{on}}{R_a})\frac{\pi^2}{8} \quad (4)$$

The best NF is obtained when R_{on} is null. In this case *NF* = 0.9 dB. With the four paths architecture, very low-noise figure can be achieved.

III. MATLAB SIMULATION RESULTS

A. System level architecture

Using the Matlab Simulink software package [7], we have simulated the four phase down sampling mixer represented in Fig. 3. The simulation takes into account the phase noise of the sampling signal V_{LO}, the switch thermal noise and the presence of radio interferences and blockers at the mixer input. The radio frequency signal V_{RF} parameters have been chosen as follow: carrier frequency f_0 = 2.4 GHz, 16-QAM modulation and 9MHz RF bandwidth. The cut-off frequency is f_C = 20 MHz and the duty-cycle is D = 0.25. The sampling signals V_{LO} are generated from a 4.8 GHz external signal.

B. Ideal transmitted signal

Fig. 4 shows the received signal constellation for an ideally 16-QAM modulated signal without any source of perturbation added. The rotation of the constellation is due to the delay produced by the time constant τ of the receiver. This problem is not harmful and can be compensated by some calibration methods.

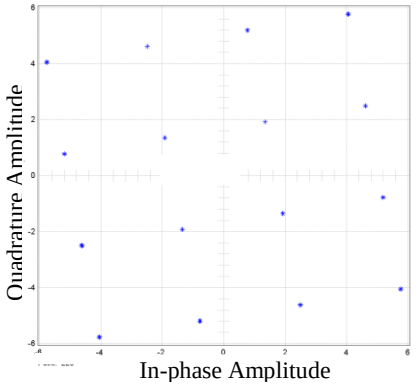

Figure 4. Ideal received constellation at the sampler output

C. Phase noise

The presence of phase noise in the sampling signal V_{LO} is a very important problem because it can degrade SNR at the output of the receiver and makes harder to detect the correct symbols. Simulations were performed with a phase noise of -102dBc@1MHz (1ps jitter). This is the maximum noise tolerated by the WiFi system. Fig. 5 shows the received constellation. Phase noise introduces some variations in the phase of received symbols which span an arc around its ideal value. Nevertheless the distortion is acceptable and received symbols still can be detected.

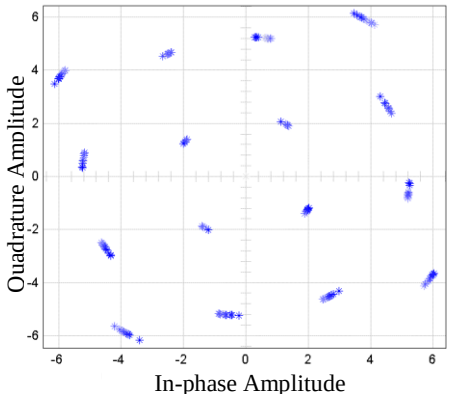

Figure 5. Received constellation with 1ps jitter@2.4GHz

 ISBN: 978-1-61208-193-9

D. Influence of the thermal noise

Fig. 6 shows the effect of the receiver's thermal noise generated by the antenna and the switch resistances. By taking R_a = 50 Ω and R_{on} = 100 Ω, NF is about 5.68 dB for 20 MHz bandwidth. The noise power at the switch output is -95.3 dBm. Here we assume 10 dB of SNR at the output, which is 10 dB lower than the expected one for a correct 16-QAM demodulation. In Fig. 6 we can observe clouds of symbol randomly distributed around the ideal one.

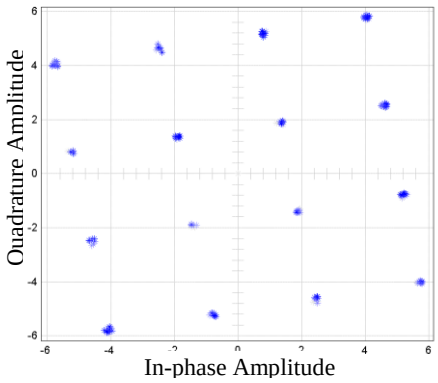

Figure 6. Received constellation with input AWG noise

E. Influence of interferers

Selectivity is one of fundamental criteria for a receiver and determines how much strong power blockers it is able to receive without deteriorating the Bit Error Rate (BER). Here we placed a sinusoidal interferer at a distance of 50 MHz from the modulated signal. The interference signal power is 10 dB higher than the power of the modulated signal. In Fig. 7 we observe symbols distributed on a circle around the ideal symbol position. This phenomenon is the consequence of AM to PM modulation in QAM systems. It shows the limits of the mixer for very close interferers in terms of filtering.

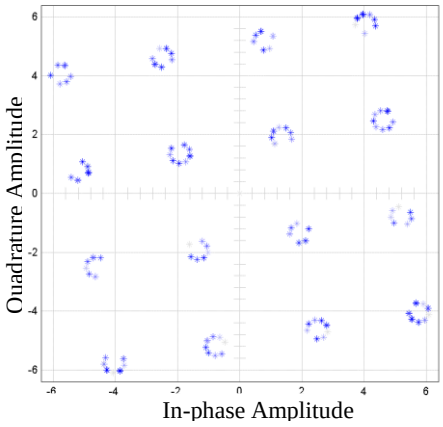

Figure 7. Received constellation with a 10dBm interferer@50MHz

That's why some passive filtering needs to be made at the antenna level. Some digital filtering can also be done on the down converted signal.

IV. Aim Of The Work

The main objective of this work is to design, realize, test and evaluate the performances of a four paths sampling mixer implemented in a 130 nm CMOS technology. The Integrated Circuit (IC), based on the structure represented on Fig. 3, includes the mixer (switches and capacitors) the four phase generator, and the low frequency amplifiers (G). The mixer is designed to work in the ISM frequency band of 868 MHz and 2.4 GHz with special care to the low power consumption. The design target IC power consumption of less than 2 mW. The finality is to demonstrate the possibility to receive different communication standards with a simple structure with low power consumption, high linearity and low noise figure.

V. Conclusion

The present article describes low complexity four paths differential sampling mixer architecture. The passive mixer has the property to act also as a high Q pass-band filter. The mixer is flexible in frequency and achieves good linearity. It consumes low dynamic power, has low noise figure and is easy to integrate on silicon. It is a serious candidate for future SDR receivers and cognitive radio applications. Some Matlab simulation results are presented in the paper. A 130 nm CMOS integrated circuit implementing the mixer and the phase generator is under development. It is dedicated to be used in the 868 MHz and 2.4 GHz ISM frequency bands.

References

[1] A. Abidi, "RF CMOS Comes of Age", IEEE Journal of Solid-State Circuits, Vol. 39, No. 4, April 2004.

[2] L.E. Franks and J.W. Sandberg, "An alternative approach to the realization of network transfer functions : the N paths filter", The Bell System Technical Journal, vol. 39, pp. 1321-1350, September 1960.

[3] M. Soer, E. Klumperink, Z. Ru, F. van Vliet and B. Nauta, "A 0.2-to-2.0GHz 65nm CMOS Receiver without LNA achieving >11dBm IIP3 and <6.5 dB NF", In: IEEE International Solid-State Circuits Conference, ISSCC, San Francisco, U.S.A., 8-12 February 2009.

[4] C. Andrews and A. Molnar, "Implications of Passive Mixer Transparency for Impedance Matching and Noise Figure in Passive Mixer-First Receivers", IEEE Transactions on Circuits and Systems-I: Regular papers, Vol. 57, No. 12, December 2010.

[5] "Discrete-Time Mixing Receiver Architecture for RF-Sampling Software-Defined Radio", IEEE Journal of Solid-State Circuits, Vol. 45, No. 9, September 2010.

[6] G. Wegmann et al. , "Charge injection in analog MOS switches", IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 6, December 1987

[7] Matlab, "The Wath Works", version 7.1.11, August 2010

 ISBN: 978-1-61208-193-9