A Novel DDS-PLL Hybrid Structure to Generate the LFM Signal

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***Abstract*—The signal generator with Direct Digital Synthesizer Phase Locked Loop (DDS-PLL) Hybrid structure generates the signal with the qualities of the wide bandwidth and high frequency resolution. The long acquisition time in the PLL limits its applications. A novel generator structure is proposed by adding the sweeping voltage circuitry to the classical DDS-PLL Hybrid in order to accelerate the acquisition speed. A test circuitry is designed to testify the novel structure. The measured results indicate that the acquisition time is reduced to be 2.175μs and 1.032μs corresponding to 1MHz and 2MHz loop bandwidth respectively; the pulse compression result is very good where the main lobe width remains as ideal, Peak Side Lobe Ratio (PSLR) is better than -38dB, and the Integrated Side Lobe Ratio (ISLR) is better than -9.5dB.**

Keywords:* *DDS-PLL Hybrid; Frequency Sweeping; Fast-locking.

I. INTRODUCTION

With the developments of radar application, the requirements of fast frequency hopping increase. It has considerable benefits to improve the radar performances and reduce the difficulties in signal processing if the signal has large bandwidth, good frequency linearity and low harmonics [1].

Generally, a signal can be generated in three ways: Phase Locked Loop (PLL) [2], Direct Digital Frequency Synthesizer (DDFS) [3] and Direct Digital Waveform Synthesizer (DDWS) [4]. DDFS is named DDS for short usually. The PLL technique operates from audio frequencies up to millimeter waves and the bandwidth is large, it also has some drawbacks: poor linearity in the frequency modulation rate, long acquisition time, and large phase error. The DDS and DDWS both operate in digital way. Although they has the advantages of fine resolution, fast switching and continuous phase, the disadvantages of serious spur and harmonics and small bandwidth are obvious. For the most advanced commercial DDS circuit, the bandwidth is less than 1.4GHz, the phase noise is better than -128dBc/Hz, and the frequency resolution is 190pHz [5]. The system speed limitation causes the bandwidth of the signal generated by the DDWS to be relatively narrow, only 400MHz most [6].

In the DDS-PLL Hybrid structure, the DDS generates the narrow-band Intermediate Frequency (IF) signal with low intermediate frequency. The PLL up converts the IF to the required RF signal and expands the bandwidth. This structure has the benefits both from the DDS and PLL.

The acquisition time is the most serious problem in the DDS-PLL Hybrid structure. In the paper, we propose a novel structure by adding a sweeping voltage circuitry to the classical DDS-PLL Hybrid structure. It brings in the benefits of shortening the acquisition time. Meanwhile, the predistortion is employed to depress the static phase error and improve the pulse compression qualities.

The remaining sections of this paper are arranged as follows. Section II analyzes the acquisition process. The novel structure is introduced in section III. Section IV lists the measurements to the signals generated by the test system in the fields of acquisition time and pulse compression. This conclusion and future work are in Section V.

II. ACQUISITION ANALYSIS

The classical DDS-PLL Hybrid structure is depicted in Figure 1. In the structure, the BPF is band-pass filter, the PD is Phase Detector, and the LF is low-pass filter. The DDS generates the signal, used as the PLL reference, with the frequency f_c. The frequency of the system clock is f_r. The PLL outputs the signal with the frequency f_0. The inherent filter in the PLL depresses the harmonics in the DDS output. The PLL multiplies the reference frequency by N to get the signal with the high radio frequency and large bandwidth [7][8][9].

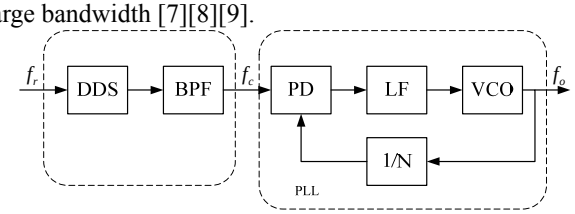

Figure 1. The Classical DDS-PLL Hybrid Structure

The process of bringing a loop into lock is called acquisition. In Charge-Pump Phase-Locked Loops (CPPLL), the process of acquisition is divided to two parts, frequency pull-in process and phase acquisition process. Pull-in tends to be slow and often unreliable. When the signal was applied, a beat note at frequency $\Delta\omega$ appears. The frequency pull-in process initiates and the beat note decreases. After the frequency pull-in process, the beat note reaches the pull-in limitation, and phase acquisition process starts. The time from unlocked state to locked state is named acquisition time. It is also divided into be frequency pull-in time and phase acquisition time. In theory, they are defined as follows for a 2nd order type 2 PLL, respectively [10].

$$T_f = \frac{\omega_r}{2\pi\omega_n^2} + \frac{2\xi}{\omega_n} \quad (1)$$

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$$T_\theta = \frac{5}{\xi \omega_n} \quad (2)$$

Where ω_r is the phase detecting frequency, ω_n is the nature frequency, and ξ is the loop damping ratio. For example, when the phase detecting frequency is 20MHz, the loop damping ratio is 0.707, and the natural frequency is 500 kHz, then the frequency pull-in time and phase acquisition time are 2.48μs and 2.25μs respectively. In general, the phase acquisition process is faster than the frequency pull-in process.

III. FAST ACQUISITION

There are some drawbacks in the classical hybrid structure namely large phase error in the steady state and long acquisition time. We propose a novel structure by adding sweeping voltage controlling circuitry to the classical structure. The novel structure is shown in Figure 2.

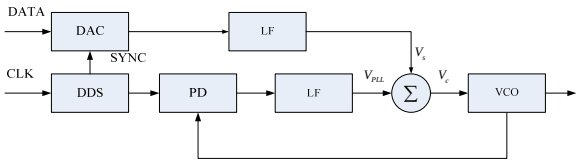

Figure 2. The block diagram of the novel topology

The CLK is the system clock. The VCO controlling voltage V_c is a sum of the sweeping voltage V_s from Digital-to-Analog Converter (DAC) and the fine-tuned voltage V_{PLL} from the PLL. The sum is realized by a voltage summer.

$$\begin{aligned} f_o(t) &= K_{VCO} \cdot V_c(t) \\ &= K_{VCO} \cdot (V_s(t) + V_{PLL}(t)) \\ &= K_{VCO} \cdot V_s(t) + K_{VCO} \cdot V_{PLL}(t) \\ &= K_{VCO} \cdot k \cdot t + K_{VCO} \cdot V_{PLL}(t) \end{aligned} \quad (3)$$

From (3), we know that the sweeping voltage is a linear function of time. A short pull-in time can be achieved since the output frequency is directly set by the controlling voltage V_c, therefore, the beat note between the divided output and reference input is smaller than the pull-in limitation $\Delta\omega_p$. The sweeping voltage takes the role of frequency setting. The phase acquisition is accomplished by the PLL. The ideal sweeping voltage curve is shown in Figure 3(a) where the sweeping voltage increases from 1.6V to 9.1V in 100μs as a straight line, and decreases to 1.6V abruptly at the end of the signal pulse. The fine-tuned voltage output by PFD is shown in Figure 3 (b) where the fine-tuned voltage varies fast in a small range of -0.1V~0.1V. Obviously, two oscillations occur in Figure 3 (b). The first one is the tracking process of the Linearity Frequency Modulation (LFM) signal from 0μs to 100μs. The second one is the process of tracking the falling frequency corresponding to the voltage falling at 100μs in Figure 3 (a). Although the instantaneous frequency migration is very large, thanks to the sweeping voltage which sets the output frequency of VCO primarily, the fine-tuned voltage converges to zero smoothly.

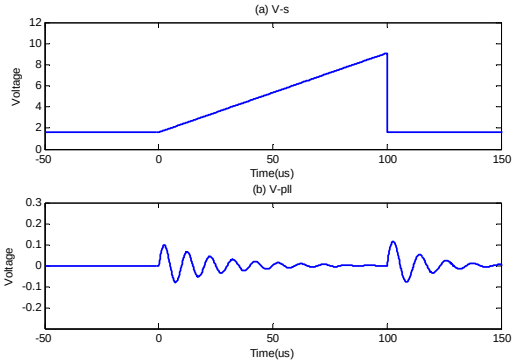

Figure 3. Simulated transient settling behavior

However, the actual voltage–frequency characteristic is nonlinear in practice. For instance, the VCO characteristic curve of ROS-2800-719+ is shown in Figure 4.

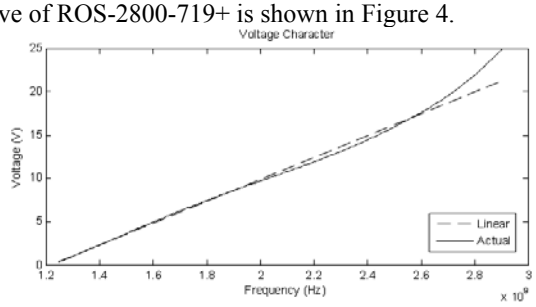

Figure 4. Characteristic of VCO

The dashed curve shows the ideal characteristic. The solid line figures out the actual VCO voltage–frequency characteristic. It approximates to a straight line in the range of 1V to 25V. The nonlinearity is serious when the voltage beyond 25V. We must note that the range with good linearity should be used when generating signals with the device ROS-2800-719+.

To sweep with the actual voltage characteristic we need to sample the actual controlling voltage and store them in the memory. The actual sweeping voltage is generated by DAC with the sample data. Synchronization of the sweeping voltage and the reference is most important. For this reason, the controlling signal SYNC is introduced as shown in Figure 2.

In the novel structure, the sweeping voltage takes the original beat note between the down-scaled frequency and the reference frequency into the pull-in limitation $\Delta\omega_p$. The frequency pull-in time is reduced to be sufficient small that we can neglect it as compared to the phase acquisition time. So there is phase acquisition time only. The acquisition speed is increased substantially.

The loop filter and summer are shown in Figure 5. The in-phase follower and RC devices in the dash frame compose the active loop filter. The PLL is 3rd order type 2. Different from the ideal 2nd order type 2 PLL, there is an

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adding high frequency pole. The influence to the transient induced by the additional pole is small. The PLL approximates an ideal 2nd order type 2. The current I_p output by the PFD is imported into inverter phase adder across the in-phase follower with the sweeping voltage across the RC filter. The summer outputs the final control voltage V_c.

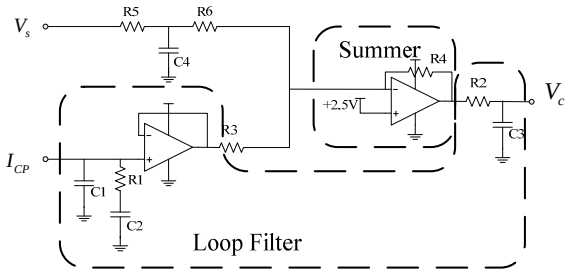


Figure 5. The loop filter and summer

The values of the components in the loop filter are listed in Table . The software ADIsimPLL provided by ADI can be used to calculate the acquisition time based on listed values.

IV. MEASUREMENT

We test the novel structure with four modules on hand. They are the DDS module, the DAC module, the filter and summer module, the PFD and VCO module. The connections and the actual circuit are shown in Figure 6.

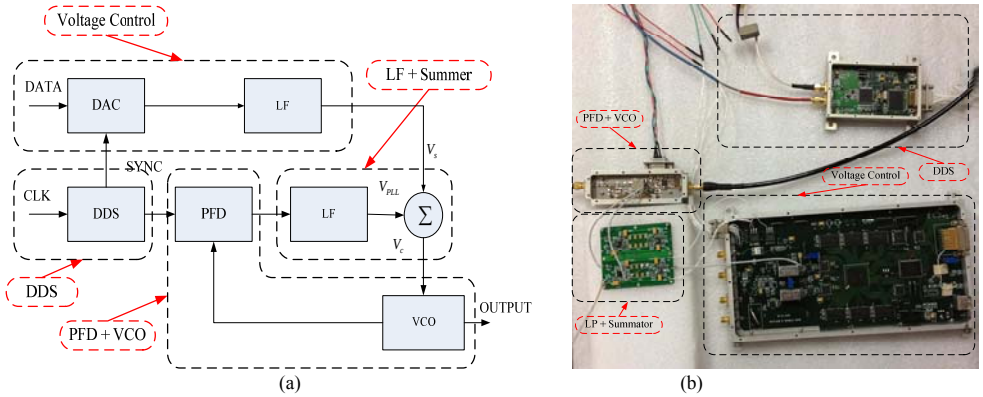
- The DDS module: The DDS we used is AD9910 with 1GSPS internal clock speed and up to 400 MHz analog outputs. There is an integrated RAM which can be used as the storage of the phase predistortion data;
- The DAC module: The DAC5675 gets 14-bits data widths, up to 400MSPS updating speed. When the SYNC comes, voltage sample data is read out from the storage, and delivered to DAC to generate the sweeping voltage;
- The filter and summer module: This module contains an active filter and an inverse summer. The circuit is as in Figure 6. The amplifiers in the filter and summer are OP1177 and AD823 respectively;
- The PFD and VCO module: The PFD is ADF4113 with the features of 0.2GHz ~4.0GHz RF input frequency, 200MHz phase detect frequency, and max 5mA current output. VCO is ROS-2800-719+ with 1.4GHz~2.8GHz output.

By changing the RC values in the loop filter, we build PLLs with 1MHz and 2MHz loop bandwidth respectively. The signal is generated with 600MHz bandwidth, 100μs pulse width, and 6MHz/μs FM rate. And the output signal is in the range of 1350MHz~1950MHz, the frequency resolution is 5.82Hz. We record the waveform by the oscillograph of DPO71254 with 6.25GHz sample rate.

The measurement of the acquisition time is difficult because the lock-in point is not easy to be determined. In this paper, we fix the lock-in point with the phase error. If the phase error falls into the range of ±10°, starts to oscillate in a small range, and diminishes, we define the loop is locked in. Based on this assumption, the phase errors of the loop with 1MHz and 2MHz bandwidth are drawn in Figure 7 and Figure 8. The red one is the phase error of the waveform, and the black one is the high-order polynomial curve. We zoom in on the starting part in Figure 7 (a) and Figure 8 (a) and show in Figure 7 (b) and Figure 8 (b).

Table I. VALUE OF COMPONENTS IN THE LOOP FILTER

Loop bandwidth	R1(Ω)	R2(Ω)	R3(Ω)	R4(Ω)	R5(Ω)	R6(Ω)	C1(F)	C2(F)	C3(F)	C4(F)
2MHz	164	1k	500	1k	500	500	50.4p	1.36n	28.4p	28.4p
1MHz	81.9	1k	500	1k	500	500	2.2p	5.45n	56.8p	56.8p
500kHz	40.9	1k	500	1k	500	500	8.7n	21.8n	114p	114p



(a) (b)

Figure 6. The test circuitry

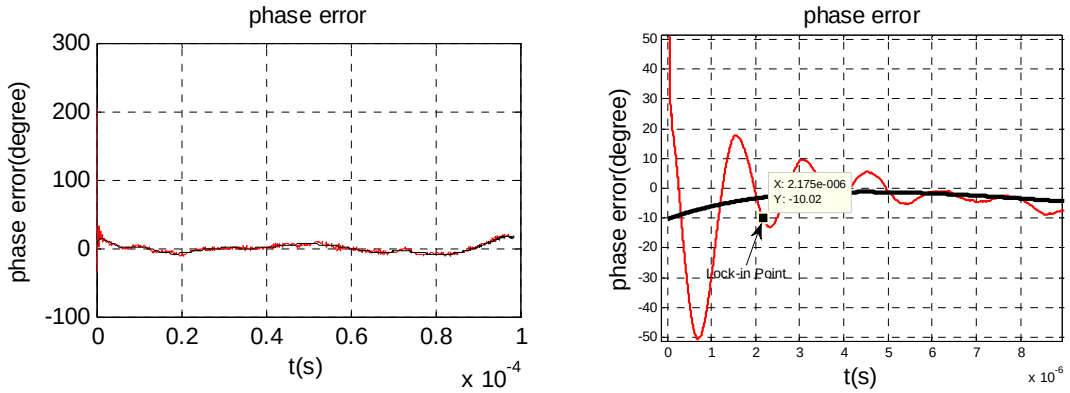


Figure 7. Locking-in time in 1MHz loop

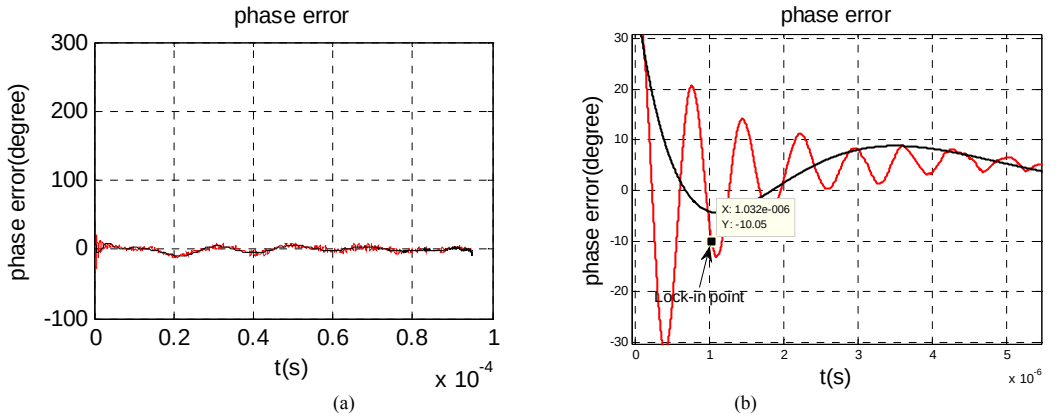


Figure 8. Locking-in time in 2MHz loop

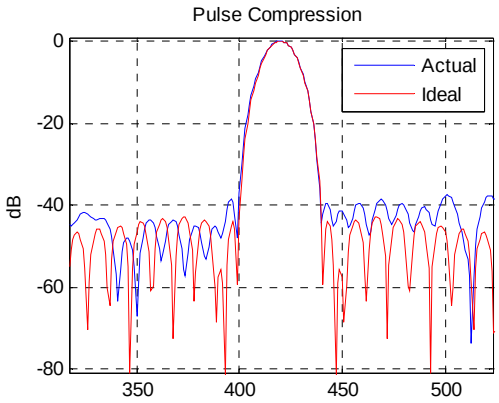


Figure 9. Compression result

In the figures, the phase error is very large at the beginning, and then diminishes quickly. We find the lock-in point and mark it in Figure 7 (b) and Figure 8 (b). The acquisition times can be read out from the figures: 2.175μs and 1.032μs for the two loops of different bandwidth respectively. We calculate the acquisition time for the classical structure using ADIsimPLL. The phase acquisition time and frequency pull-in time are 3.43μs and 2.32μs for the loop of 1MHz bandwidth. And they are 2.175μs and 1.032μs for the loop of 2MHz bandwidth. Obviously, the total acquisition time is decreased to approach phase acquisition time. The novel structure proposed in this paper is effective to reduce the frequency pull-in time.

The pulse compression with Hamming weight is shown in Figure 9. The red curve is the pulse compression with ideal signal; the blue curve is the pulse compression with the actual signal. It has perfect

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performance. The main-lobe width of the actual signal is the same as the ideal one, the PLSR is better than -38dB, and the ISLR is -9.5dB towards -9.9dB for the ideal.

V. Conclusion and Future Work

A structure of fast locking signal generator is proposed in this paper, with adding sweeping voltage circuitry to the classic DDS-PLL Hybrid. Great decrease of the frequency pull-in time is achieved because the PLL is brought in the pull-in range by the sweeping voltage. To validate the structure, a test system is built to generate a LFM signal with 600MHz bandwidth, 100μs pulse width and 6MHz/μs FM rate. The acquisition time is reduced to be 2.175μs and 1.032μs with 1MHz and 2MHz loop bandwidth respectively. Based on this novel structure, signals with wider bandwidth and longer duration are expected to be generated to improve the qualities of radar.

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