A Method to Determine the Static NBTI Stress Time of an Embedded Component in an Integrated Circuit

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Abstract—**This paper presents a simple mechanism to accurately estimate the number of clock cycles that an integrated circuit (IC) has operated. It is achieved by measuring the delay of an embedded component due to static negative bias temperature instability (NBTI) effects. Simulations with the HSPICE tool, using 45nm predictive technology model and a NBTI degradation model are presented. The results also indicate that using static NBTI aging model aides in very early stress time detection.**

Keywords-Negative bias temperature instability (NBTI); counterfeit; aging; odometer; built-in self-test (BIST).

I. INTRODUCTION

When a circuit operates, there are changes in certain characteristics which are used in this work in order to determine its operating time. As Complimentary Metal-Oxide Semiconductor (CMOS) technology is shrinking, Negative Bias Temperature Instability (NBTI) was attributed as one of the major causes of changes in circuit characteristics in digital circuits. The NBTI degradation causes an increase in the threshold voltage of a P-type Metal-Oxide Semiconductor (PMOS) transistor and consequently decreasing the transistors drain current and transconductance over time [13]. NBTI is attributed to the creation of interface traps and oxide charges by a negative bias voltage on the gate of the transistor at elevated temperatures. Typically, the stress temperature lies in the range of 100-250°C and the oxide electric fields below 6 MV/cm. Such conditions occur during the burn-in test and normal operation of high performance machines [12]. The threshold voltage of PMOS transistors degrades and this may alter temporal characteristics of a chip.

The focus of this study is to derive an estimate of the number of clock cycles that the integrated circuit (IC) has operated. It is determined by measuring delays due to static NBTI effects. Several models [3][6][14][15][17][18] have been introduced to determine the degradation of the threshold voltage due to NBTI effects. The authors in [17] provide a general framework to analyze NBTI degradation while taking into consideration various circuit parameters like supply voltage, temperature, node switching activity, input patterns, and the duty cycle. The work in [6] introduced an analytical model for dynamic NBTI aging of PMOS transistors based on the Reaction-Diffusion (R-D) model framework. Meanwhile, the authors in [3] and [14] introduced an analytical predictive model for static and dynamic NBTI aging of PMOS transistors based on the reaction-diffusion mechanism of the atoms. They provided an accurate threshold change due to static NBTI aging. However, they only provided upper bounds on the threshold change due to dynamic NBTI aging because the intent was to apply the approach in timing analysis. The authors in [18] presented a framework to analyze the impact of NBTI degradation on circuit performance under various operating conditions such as temperature and frequency. The authors in [2] presented a model to monitor delay on paths in the presence of NBTI aging and process variation. The authors in [7][8][9] considered the effect of hole trapping and interface-state generation to develop an accurate analytical model to identify the threshold voltage degradation due to NBTI. The work in [15] introduced a unified aging model of NBTI and HCI degradation for MOSFET circuits. Their model considers NBTI and HCI effects together to indicate the degradation in threshold voltage at a given time.

This paper presents a built-in approach that estimates accurately the number of operational clock cycles applied to a circuit. In semiconductor industry, an odometer is defined as the instrument used to identify the age of a given circuit. The presented approach acts an odometer as it estimates the number of clock cycles that have been applied to the circuit. The approach operates under static NBTI stress whenever the system clock is enabled. The approach applies static NBTI stress (i.e., low voltage) on the PMOS transistors in a chain of inverters. This causes a change in the threshold voltage of the transistors and subsequently, the delay of the chain of the aging inverters increases rapidly. Static signals are known to age the transistor very fast and therefore the presented approach detects very early stress times. Static signals do not induce dynamic NBTI and Hot Carrier Injection (HCI) effects whose aging effects are not modeled precisely. Hence using static NBTI results into an accurate odometer approach.

The proposed method is compatible with the IEEE 1149.1 standards and does not impact the timing performance of the circuit. The presented approach will be able to identify the time for which a circuit has been used. This will also help us identify if the given circuit is counterfeit, i.e., has been used in an unauthorized manner.

A counterfeit component is defined as a component which is either an off-specification, defective, or used original component manufacturer (OCM) product sold as ‘‘new’’ or working [4]. Recycled components from circuits would operate slower and may fail to work early during their lifetime. Such recycled and remarked components jointly contribute to over 80% of counterfeit products [4]. The reliability of the product is compromised in commercial, industrial or defense applications which pose a major concern in safety critical applications, for example, defense projects and aviation industry. An application of the work is to detect counterfeit integrated chips.

The paper is organized as follows. Section II overviews existing methods to identify aging due to NBTI. Section III provides the preliminaries for the presented work. In particular, it elaborates on the predictive models for static and dynamic NBTI stress. Section IV provides the proposed built-in mechanism and details about the design. Section V provides the experimental results indicating the accuracy of the method in comparison to earlier proposed techniques. Section VI provides with concluding remarks and future work.

II. PRIOR RELATED WORK

There exist some recent NBTI based counterfeit detection methods in the literature. However, all of them rely on dynamic NBTI effects which have not been modeled as accurately as static NBTI effects. It is known that the threshold voltage does not change as rapidly as with static NBTI effects. Instead, the proposed approach uses static NBTI and therefore results into a more accurate prediction of the circuits operating time. Furthermore, dynamic NBTI effects occur concurrently with HCI effects. This complicates their application to the problem studied in this paper.

The authors in [10] consider counterfeit circuit detection without inserting any additional hardware. Two similar circuit paths that undergo dissimilar signal activity are chosen and their delay is calculated with simulations among several circuit instances. The path delays are also computed and curve fitting is done for aged circuit instances. No details are presented on the likelihood of identifying identical paths that are sensitized similarly and there are no details on the signal activity calculation. The latter is a challenging task because the activity on a path depends on the application being executed on the chip. Furthermore, intra-process variations impact the accuracy of the approach. Finding a pair of paths given all the above constraints is a very challenging problem and for some IC's one might not be able to find such a pair of paths. Finally, no results are presented on the total stress time that the PMOS transistors on the paths must undergo during the circuit operation so that the IC stress time is detected.

Another approach for counterfeit detection was recently presented in [11]. The authors use two identical copies of pass logic buffer chains. When the circuit operates, some lines undergo stress at almost every clock cycle. A line with high zero-duty cycle is selected as an input to the buffer chain. The zero-duty cycle was defined as the average time for which a signal remains zero during a clock cycle. This ensures that one of the buffer chains undergoes continuous stress whereas the other chain is kept inactive. The difference in the delays of the buffer chain indicates whether a circuit is aged or not. However, in [11] the authors proposed to take a line from within the circuit. This line needs to have a high zero-duty cycle in the range of 0.9-0.999. It is difficult to find such a line in the circuit. In particular, the zero-duty cycle of a line depends on the application being executed on the circuit. A given line may have the highest zero-duty cycle in a circuit for a specific application but low zero-duty cycle for another application. Hence, it is challenging to identify the line that minimizes the detection of the stress time. Most importantly, we observed that the experimental setup in [11] does not work for circuits that operate at a frequency greater than 1GHz. This happens due to a design flaw. At 1GHz and higher frequencies in particular, the pass logic gate buffers fail to stay open for sufficient time for the signal to cause aging on the PMOS transistor in the chain. This limits the application of the approach. The presented method does not suffer from such challenges.

The authors in [1] present an on-chip NBTI and PBTI tracking technique. Pass logic transistors are used to track dynamic NBTI aging using the model in [3]. The input to the aging sensors is either an internal critical line with the largest duty cycle or a generated signal with similar duty cycle. The objective is to adjust the circuits mode of operation (such as voltage and frequency scaling) as it ages.

The experiments were performed at room temperature but it is known that NBTI effects are pre dominant at high temperatures [13]. Our approach is different than [1] and [11] since we use static NBTI aging. Unlike dynamic NBTI effects, static signals do not cause an increase in temperature due to switching. Therefore, accurate experiments can take place using room temperature. In addition, dynamic NBTI aging is dominated by the duty cycle of the input signal of the aging circuitry which is difficult to calculate [11]. Furthermore, as noted earlier, dynamic NBTI aging should always be considered in concurrence with HCI aging, and neither [1] nor [11] consider the impact of HCI aging effects. For these reasons, [1] and [11] are not good candidates for the odometer application studied in this paper.

The work in [10] and [11] both utilize dynamic NBTI aging, which is explained in the next section. Dynamic NBTI is based on zero-duty cycle which is a very difficult

quantity to be calculated and the analysis using dynamic NBTI aging is cumbersome. The authors in [5] try to characterize the dynamic NBTI aging effect for different operating conditions. The method utilizes controlled stress conditions. They control the input frequency (in their experimentation, this amounts to controlling the temperature), as well as the zero-duty cycle of the input signal. Furthermore, they control the voltage at which the ring oscillators (ROSC) operate and the time for which the circuit will be aged. Experimental results of manufactured circuits show that dynamic NBTI aging varies greatly as a function of the temperature, even if the zero-duty cycle and other parameters are known. For all these reasons, dynamic aging is not recommended for the odometer problem studied in this paper.

III. EXISTING PREDICTIVE NBTI MODELS

Several NBTI aging models have been presented in the literature, see [3] and [6]. The change in threshold voltage (ΔV_{th}) due to NBTI aging is modeled using the Predictive Technology Model (PTM) in [3]. It is very accurate in modeling static NBTI aging. The static NBTI aging equation is:

$$\Delta V_{th} = A\left((1+\delta)t_{ox} + \sqrt{Ct}\right)^{2n} \quad (1)$$

where t is the total stress time and n is the time exponent, n = 1/6 for H_2 diffusion based model. Let $C = T_0^{-1}\exp(-E_A/kT)$ where $T_0 = 10^{-8}$, $E_A = 0.49\ eV$. Let k denotes the Boltzmann constant, i.e., $k = 1.381\times10^{-23}\,m^2kgs^{-2}K^{-1}$ and T is the temperature. Let δ = 0.5 and t_{ox} denotes the oxide thickness and is technology dependent. A is given as

$$A = \left(\frac{qt_{ox}}{\epsilon_{ox}}\right)\left(K^2 C_{ox}\left(V_{gs}-V_{th}\right)\left(\exp\left(\frac{E_{ox}}{E_0}\right)\right)^2\right)^{1/2n} \quad (2)$$

Electric field is given as $E_{ox} = \left(V_{gs}-V_{th}\right)/t_{ox}$. Let q be the electron charge. Let C_{ox} denote the oxide capacitance per unit area and is expressed as $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{\epsilon_o\epsilon_r}{t_{ox}}$

Let ϵ_o denote the permittivity of free space, its value is $\epsilon_o = 8.854\times10^{-14}F/cm$. Let ϵ_r denote relative permittivity and is $\epsilon_r = 3.9$ for SiO_2. Let $K = 8\times10^4\ s^{-0.25}C^{-0.5}nm^{-2}$ and let $E_0 = 0.335\ V/nm$

It is observed that under static NBTI stress, the temperature of the transistors does not increase since there is no switching activity. It will be shown that one can accurately estimate the number of clock cycles for which static stress is applied as long as the process parameters such as t_{ox}, V_{th} are known.

For completeness, the section also outlines the predictive model for dynamic NBTI aging, which is used in [5][10][11]. The model provides an upper bound and not necessarily an accurate estimate. The upper bound on dynamic NBTI aging was calculated using the expression below.

$$\Delta V_{ths,m+1} = (K_v^2\alpha T_{clk})^{2n}\left(\sum_{i=1}^{m}\left(\underline{\prod_{j=m-i+1}^{m}\beta_t^{1/2n}}\right)\right)^{2n} \quad (3)$$

$$\Delta V_{ths,m+1} = (K_v^2\alpha T_{clk})^{2n}\left(\underline{\sum_{i=1}^{m}(\beta_t^{1/2n})^i}\right)^{2n} \quad (4)$$

The underlined term in (3) and (4) was estimated as $(\beta_t^{1/2n})^i$ and $\frac{1}{1-\beta_t^{1/2n}}$ respectively which provides the upper bound. It is important to focus on an accurate NBTI aging model since the goal is to precisely identify the time for which the circuit has been used.

$$\Delta V_{th} \le \left(\frac{\sqrt{K_v^2\alpha T_{clk}}}{1-\beta_t^{1/2n}}\right)^{2n} \quad (5)$$

The change in the threshold voltage due to dynamic NBTI aging is given by (5) [3]. The dynamic NBTI model considers various parameters to determine the effect on threshold voltage due to NTBI aging namely duty cycle (α), temperature (T), oxide thickness (t_{ox}) and gate to source voltage (V_{GS}) as shown in the equations below. From [11] it was observed that dynamic NBTI aging is very sensitive to α. Calculating α for embedded lines in an IC is a challenging problem.

$$\beta_j = 1 - \frac{2\xi_1 t_e + \sqrt{\xi_1 C(1-\alpha)T_{clk}}}{2t_{ox} + \sqrt{CjT_{clk}}} \quad (6)$$

$$C = T_0^{-1}\exp(-E_A/kT) \quad (7)$$

$$K_v = \left(\frac{qt_{ox}}{\epsilon_{ox}}\right)^3 K^2 C_{ox}\left(V_{gs}-V_{th}\right)\sqrt{C}\exp\left(\frac{2E_{ox}}{E_0}\right) \quad (8)$$

For these reasons, it is a cumbersome task to use dynamic NBTI aging as a method to predict the number of clock cycles that the circuit has operated.

IV. THE PROPOSED APPROACH

The proposed method inserts two identical chain of inverters in comparison to the pass logic transistors used in [11]. One of the chain ages while the other does not. When a test signal is applied to both chains, the delay difference is measured. This delay is sufficiently large enough that it can be easily detected at a very early time. Then the proposed odometer method uses a pre-determined relation of observed delay vs. static NBTI stress time in order to identify the number of operating clock pulses in the design, i.e., the age of the circuit.

As stated earlier, the proposed approach consists of embedding two inverter chains. One chain will experience static NBTI stress and age rapidly. Let this chain be denoted as AC_s. The other chain will not age and will only be activated during testing. Let this chain be denoted as NAC_s. The delay of the AC_s changes due to the static NBTI when compared to the delay of the NAC_s. This AC_s delay is increasing as a function of the static stress time. A built-in approach that is capable of detecting a delay on the AC_s no less than 12.803ps in 45nm technology with V_{gs}=1.9 V and T = 300 K is presented.

Then the odometer method is based on Figure 1 which shows the correlation of the AC_s delay to the static NBTI stress time. The relationship depicted in Figure 1 is very accurate for the following two reasons. First, the ΔV_{th} calculation in (1) is very accurate given that the mentioned constants and $t_{ox} = 1.3nm$, $V_{gs} = 1.9\ V$ are used. The t_{ox} is technology specific and V_{gs} is decided by the designer hence these values can be easily extracted. Secondly, there are mainly two process parameters that may affect the accuracy namely the oxide thickness t_{ox} and temperature T. Since the use of static NBTI stress, the approach is unaffected by the temperature. For t_{ox}, using simulations, it has been verified that the change in ΔV_{th} is very negligible to cause any significant deviation from the ideal inverter delay shown in Figure 1. Thirdly, there are other fabrication parameters that might cause variations but the two inverter chains are so closely placed, such that those variations will cancel out and will not affect the accuracy of the presented approach. Even though the work in [10] was unaffected by intra-die process variations, it was not immune to the process parameters t_{ox} and T.

When a circuit is activated the clock is applied to the respective module of the circuit based on the application executed on the chip. Hence, a circuit has been aged for as long as the clock is applied. Thus, it is proposed to use the clock signal to monitor the age of the circuit. It is known that static NBTI aging causes the most rapid degradation in the threshold voltage. Hence, the proposal is to generate a static zero signal using the clock of the circuit.

A combination of an AND gate (G2) and an inverter (G1) is used as shown in Figure 2. The system clock signal and its inversion are given as input to the AND gate. Due to the AND gate properties, a constant zero signal is generated. The delay introduced due to the inverter causes very small glitches in the generated signal. The glitches do not reach sufficiently high voltage to switch the state of the transistor. Hence, the glitches are not a problem and the transistor is constantly stressed.

This static zero signal will be an input to stress time detection module (STDM). The STDM consists of two

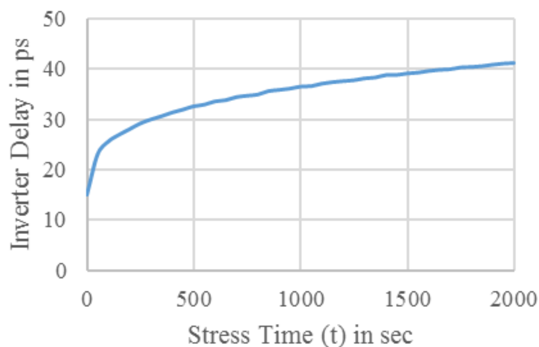

Figure 1. AC_s detected delay due to applied static NBTI stress.

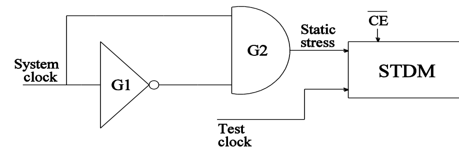

Figure 2. Static zero generation using system clock signal.

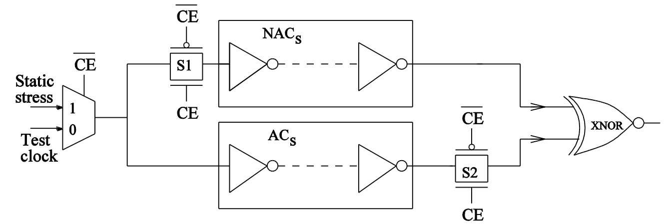

Figure 3. The schematic of STDM.

similar chain of inverters embedded on the chip which are placed very close to each other as shown in Figure 3. Hence, the two inverter chains are unaffected by intra-die process variations. One of the inverter chain experiences static NBTI stress. Let us call this chain as Static Aging Chain (AC_s) while the other is only enabled during the testing phase. Let us call this inverter chain as Static Non-Aging Chain (NAC_s). There is a multiplexer to control the input to the two the NAC_s and AC_s chains. The multiplexer during normal operation of the IC lets the static signal through and lets through the test clock during the test phase depending on the current mode of operation controlled by circuit test enable signal ($\overline{CE}$). There is a XNOR gate to detect the delay between the NAC_s and the AC_s. During the normal operation of the circuit, the NAC_s is isolated from aging using a pass logic transmission gate S1 meanwhile S2 isolates the XNOR from aging.

During normal operation of the circuit, $\overline{CE}$ is 1. Thus, switches S1 and S2 are closed and the static stress input only ages the AC_s. Meanwhile, the NAC_s is not aging at all. During the test mode, $\overline{CE}$ is switched to 0 hence, the test clock signal is applied to the STDM. This test clock signal can be chosen as the system clock or any signal as per the designer. During experimentation, it was assumed as the system clock. Since $\overline{CE}$ is now 0, the switches S1 and S2 are open and the test clock signal is applied to the NAC_s and AC_s. This signal propagates through the two chains. The NAC_s signal is going to arrive earlier than the AC_s signal due to the aging induced in the AC_s. The XNOR will identify the delay between the two chains and produces a pulse proportional to the delay between NAC_s and AC_s. This pulse can be observed at the output pin of the chip. There are many techniques in the literature that can be used to detect on-chip delay of paths for example [16]. But having a dedicated pin will help us provide more information about the chip in the future.

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V. EXPERIMENTAL RESULTS

Experimental results have been evaluated on some of the largest ISCAS'89, ITC'99 benchmarks. Experiments were conducted on a Linux machine with Intel Xeon 6 core @ 2.40GHz processor and 23GB memory. The first transistor in the chains is minimum sized. The PMOS size is $(W/L)p=(0.24U/0.045U)$, while the NMOS size is $(W/L)n=(0.12U/0.045U)$. Successive inverters are sized using appropriate sizing techniques. HSPICE [20] simulations are performed by using predictive PTM 45nm technology library [19].

Firstly, the experiments were performed using a single inverter, which experienced static NBTI aging. The PMOS and NMOS sizes used for this inverter are as mentioned above. The earliest detection time for static NBTI stress was found to be 30 days which is an unreasonable static NBTI stress detection time. To facilitate a much earlier detection, an inverter chain consisting of 100 inverters was used. It was necessary to use such a substantial number of inverters because only half of the inverters will be stressed. This is due to the inversion of the signal and the fact that NBTI aging occurs only on the PMOS transistors.

The experiments were repeated and it was found that the earliest detection time using the 100 inverter chain was reduced from 30 days to 2 seconds. The corresponding delay was observed to be 12.803ps. One can either choose an earlier detection time or reduce the hardware overhead and have a late detection time. But choosing a later detection time may leave your IC's integrity vulnerable.

Experiments were performed on some of the important benchmarks. The ISCAS'89, ITC'99 benchmarks were used in order to compare the results of the presented approach to [10]. Table I lists the earliest detection time for the proposed approach and [11] with different zero-duty cycle (ζ) observed for the known ISCAS'89, ITC'99 benchmarks. The work in [5] was excluded from the comparison below since it does not work for high frequency circuits and the work in [10] since it does not calculate the earliest stress detection time. Column 1 lists the approaches and various ζ values for [11]. Column 2 in Table 1 lists the earliest detection time observed for the two approaches. Column 3 lists the benchmarks which have the property of having a single line with the ζ mentioned in Column 1.

In particular, row 1 shows that the earliest detection time for static NBTI aging is 2 seconds. This detection time holds for any given circuit because the proposed approach is based on the static NBTI stress generated using the system clock. Row 2 presents the earliest detection time for the approach using [11] and ζ=0.997. Using input zero probability 0.5 and simulations showed that the circuits b15 and s15850 from the ITC'99 and ISCAS'89 collections, respectively, have a line with ζ approximately 0.997. Thus, the earliest detection NBTI stress time for each of these two circuits is approximately 72.3 hours.

The improvement over [11] becomes even more pronounced for circuit b20 from the ITC'99 collections

TABLE I. COMPARISON OF EARLIEST DETECTION TIME FOR BENCHMARKS USING PROPOSED APPROACH AND [11]

<table>
<tr><th colspan="2"></th><th>Earliest Detection Time</th><th>Benchmarks</th></tr>
<tr><td colspan="2">Proposed Approach</td><td>2sec</td><td>Any</td></tr>
<tr><td rowspan="4">[11]</td><td>ζ=0.997</td><td>72.3h</td><td>b15, s15850</td></tr>
<tr><td>ζ=0.984</td><td>504h</td><td>b20</td></tr>
<tr><td>ζ=0.981</td><td>528h</td><td>b22</td></tr>
<tr><td>ζ=0.977</td><td>674h</td><td>s13207, s35392</td></tr>
</table>

where the ζ is 0.984 Column 2 shows that the earliest NBTI stress time detected using [11] is 504 hours. Likewise, it is observed that the impact of the method for circuits b22 is much more pronounced. For this circuit, the simulations showed that the ζ is 0.981 and the earliest detection time was found to be 528 hours. Meanwhile, for s13207 and s35392 the ζ was found to be 0.977 and the earliest detection time was found to be 674 hours. All these results show that the proposed approach is significantly better among the two.

Adding 200 inverters might seem like a huge hardware overhead hence a simple study to identify the hardware overhead was performed. The total number of transistors for the ISCAS'89, ITC'99 benchmarks reported in Table III were calculated using the transistor count of individual gates and flip-flops present in the benchmarks. Table II lists the transistor count of the different gates present in the reported benchmarks. Column 1 lists the type of the gate or component. Column 2 lists the number of transistors present in the respective gate or component.

Table III lists the hardware overhead of the proposed approach on select ISCAS'89, ITC'99 benchmarks. Column 1 lists the benchmarks that were used to measure the hardware overhead. Column 2 provides the total number of transistor in the given benchmarks. Column 3 lists the overhead percentage of the proposed approach. It is observed that the hardware overhead of the complete approach is less than 0.54% for some of the biggest ITC'99 benchmarks. Even for the smaller benchmarks like b15, s15850, and s13207, the hardware overhead is less than 1.26%. This proves that the proposed method provides a significant improvement over existing approaches as well as minimizes the hardware overhead for such a challenging problem formulation.

TABLE II. TRANSISTOR COUNT FOR VARIOUS LOGIC GATES

Logic Gates	Transistor Count
D Flip Flop	18
AND, OR	6
NAND, NOR, BUFFER	4
INV	2

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TABLE III. HARDWARE OVERHEAD OF THE PROPOSED APPROACH

Benchmarks	Total number of transistors	Overhead (%)
s13207	36646	1.26
s15850	41900	1.1
b15	42396	1.09
b20	86340	0.54
s35392	98138	0.47
b22	128600	0.36

VI. CONCLUSIONS

A method for the earliest identification of the delays due to static NBTI stress is proposed. The approach uses inverters that age at each application of the system clock. The experimental results show that the approach detects static NBTI aging very early in the lifetime of a circuit. The method can be used as an odometer for the life cycle of the circuit independent of its operating frequency. The approach has negligible built-in hardware overhead.

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