Prototype Design of Computationally Efficient Digital Down Converter for 3G Applications

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Abstract— **This paper presents Digital Down Converter (DDC) design for Software Defined Radio (SDR) base stations using reconfigurable logic. A computationally efficient multistage design technique is used to achieve an efficient solution for third generation (3G) mobile communication. The proposed design is developed in three stages and each stage has been optimized using Park McClellan algorithm to minimize the filter order. This was further supplemented with computationally efficient polyphase decomposition technique. The Partially Serial Pipelined MAC algorithm is used to optimize both speed and area simultaneously. The embedded multipliers of target Field Programmable Gate Array (FPGA) are optimally utilized and efficiently mapped to enhance the system performance. The proposed DDC has shown an improvement of 19 % in speed with improved resource utilization to provide a computationally efficient and cost effective solution for SDR based wireless applications.**

Keywords-3G Mobile Communication; Base Stations; Radio Transceivers; Reconfigurable Logic; Software Radio.

I. INTRODUCTION

Digital Signal Processors (DSPs) are specialized devices designed to implement digital signal processing algorithms on a stream of digitized signals. The highly competitive nature of the wireless communications market and constantly evolving communication standards have resulted in short design cycles and product lifetimes. This environment has led to the emergence of a new class of configurable DSPs, which can leverage hardware flexibility, programmability, and reusability, to provide highly customizable DSP solutions [1]. In the recent past, telecommunications techniques have achieved a wide popularity, mainly due to the huge diffusion of cellular phones and wireless devices. The request for more complex and complete services, such as high speed data transmission and multimedia content streaming, has moved many research groups in the electronic field towards the study of new and efficient algorithms, codes and modulations. In Software Defined Radios, most radio receiver processing functions are to be run on a general purpose programmable processor rather than being implemented strictly on non-programmable hardware. The functionality of SDR receiver processor can be changed via "software reprogramming." The concept of SDR is now an IEEE Standard, i.e., IEEE P1900 [2]. These radios are reconfigurable through software updates. For high end digital signal processing where the highest possible performance is needed at low power consumption, Application Specific Integrated Circuits (ASICs) are still the processors of choice. However, ASICs require very long design and development times and are very expensive to design and manufacture. Moreover, ASICs are inherently rigid and are not very well suited to applications that are constantly evolving. For these reasons, Programmable Logic Device like Field Programmable Gate Arrays have emerged as an alternative to ASICs in wireless communication systems.

FPGAs are mainly used for the flexibility they provide. Like programmable DSPs, FPGAs are programmed and configured in software. This makes it very easy to upgrade or add functionality to an FPGA, even if it is already deployed in the field. Like ASICs, FPGAs achieve high levels of performance by implementing complex algorithms in hardware. FPGAs are particularly well suited for accelerating algorithms that exhibit a high degree of data flow parallelism. The FPGAs suffer from the drawbacks of inefficient resource utilization, high cost and power consumption [3]. The cost factor can be improved by using less expensive FPGAs for system design and by efficient utilization of FPGA resources. The power factor can be improved by optimal usage of SRAM based programming interconnections. With increasing demand of battery dependent devices, methods for reduction of the power consumption of the memory blocks have received significant interest. Six transistor SRAM cells are preferred for many applications because of its high speed and robustness. The rest of the paper is structured as follows. Section II presents the design specifications of Wideband Code Division Multiple Access (WCDMA) DDC and related state of the art design approaches. Section III shows design simulations and structures. Hardware implementation with area and speed comparison is in Section IV and we conclude in Section V.

II. DIGITAL DOWN CONVERTER

The SDR system can change its radio functions by swapping software instead of replacing hardware, which seems to be the best solution given that mobile standards are springing up like mushrooms [5]. SDR thereby makes it possible to reprogram cell phones to operate on different radio interface standards. But that's not all. Putting much of a radio's functionality in software opens up other benefits. A mobile SDR device can cope with the unpredictable dynamic

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characteristics of highly variable wireless links [6]. SDRs use a single hardware front end but can change their frequency of operation, occupied bandwidth, and adherence to various wireless standards by calling various software algorithms. Such a solution allows inexpensive, efficient interoperability between the available standards and frequency bands [7]. Fig. 1 illustrates SDR Base Station (BS) receiver that consists of two sections – a front-end high-data rate processing section and a back-end symbol rate or chip-rate processing section.

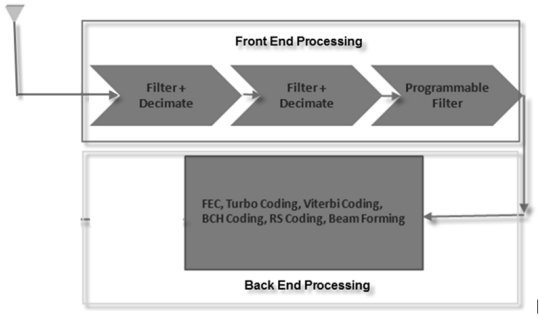

Figure 1. Reconfigurable SDR BS Receiver

Reconfigurable architectures provide flexible and integrated system-on-chip solutions that accommodate smooth migration from archaic to innovative designs, allowing recycling of hardware resources across multiple generations of the standards [8]. SDR technology enables such functionality in wireless devices by using a reconfigurable hardware platform across multiple standards. Sampling rate converters play important role in SDR systems [9]. Digital up-converters (DUCs) and digital down-converters (DDCs) are important components of every modern wireless base station design. DUCs are typically used in digital transmitters to filter up-sample and modulate signals from baseband to the carrier frequency [10]-[12]. DDCs, on the other hand, reside in the digital receivers to demodulate, filter, and down-sample the signal to baseband so that further processing on the received signal can be done at lower sampling frequencies. They are more popular than their analogue counterparts because of small size, low power consumption and accurate performance [13]-[17].

DDC performs decimation and matched filtering to remove adjacent channels and maximize the received signal-to-noise ratio (SNR) [18]. For the reference WCDMA DDC design, the carrier bandwidth is equal to 5.0 MHz, the number of carriers is 1, intermediate frequency (IF) sample rate is equal to 61.44 MSPS, the DDC output rate is 7.68 MSPS, the input precision equals 14 bits, the output precision equals 16 bits and the mixer resolution is 0.25 Hz approximately and SFDR up to 115 dB is required.

The DDC input is assumed to be real, directly coming from the Analog to Digital Converter (ADC). The mixer translates the real band pass input signal from intermediate frequency to a complex baseband signal centered at 0 Hz. Mathematically, the real input signal is multiplied by a complex exponential to produce a complex output signal with real and imaginary components. The sinusoidal waveforms required to perform the mixing process are obtained by using the Direct Digital Synthesizer (DDS). The decimators in the DDC need to down sample the IF data from 61.44 MHz back to 2x chip rate. The factor of 61.44/7.68 = 8 can be partitioned using different possible configurations. The down sampling by eight at once will result in an extremely long filter length and result in an inefficient hardware implementation. The use of shaping filter with decimation factor of 2 allows the remaining stages to be implemented as either one half band filter with decimation factor of 4 or two half band filters with decimation factor of 2 each. The second configuration is more suitable for hardware implementation because of less hardware consumption [19]-[21]. The existing designs suffer from the limitations that their implementation is based on Xilinx FIR compiler blocks and DDS compiler blocks which are based on DSP 48E/A slices. The DSP 48 E/A slice based FPGAs are costly as compared to multiplier based FPGAs and results in costly design implementation. So there is great necessity to implement DDC design on multiplier based low cost FPGA to provide an economically optimized solution in terms of area and speed, which is presented in following sections.

III. PROPOSED DDC

An efficient DDC is designed for WCDMA applications. The proposed DDC design is using three decimator stages. The input sample rate of first decimator is 61.44 MSPS, and the output sample rate is 30.72 MSPS. The pass band frequency is 2.34 MHz and the pass band ripple is 0.002 dB. It results in a digital filter of order 10 whose response is shown in Fig. 2.

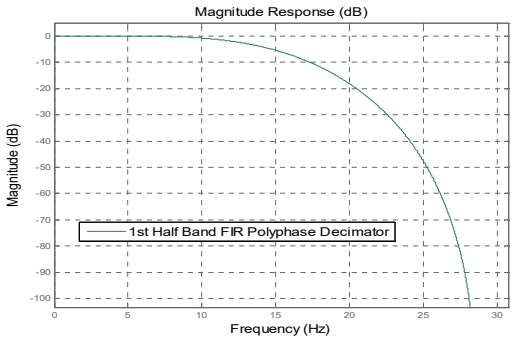

Figure 2. First Stage Half Band Decimator Response

The proposed partially serial pipelined Multiply Add and Accumulate (PSPMAC) algorithm design technique based stage 1 decimator is shown in Fig. 3. The 11 coefficients of first stage decimator have been processed by using 3 multipliers in partially serial style using MAC algorithm to optimize both speed and area factor simultaneously. The input pipeline registers are used to store the new coefficient values required for processing in the next cycle to further enhance the speed. The Cascade Enable (CE) delays are used to synchronize between stage 1 and stage 2. The pass

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band edge of second decimator is 2.34 MHz and pass band ripple is 0.0001 dB. It results in a digital filter of order 18, whose response is shown in Fig. 4.

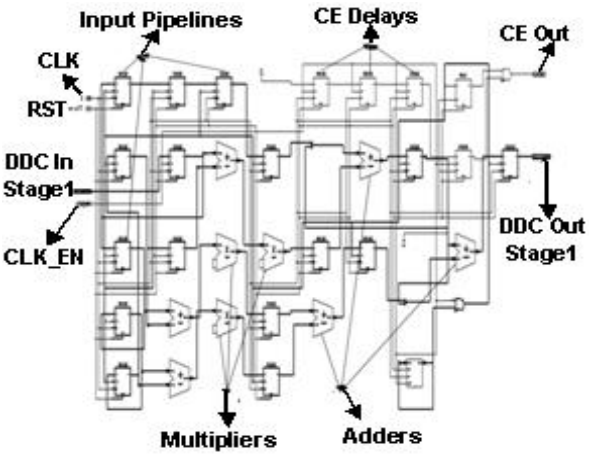

Figure 3. Stage 1 PSPMAC Based Decimator

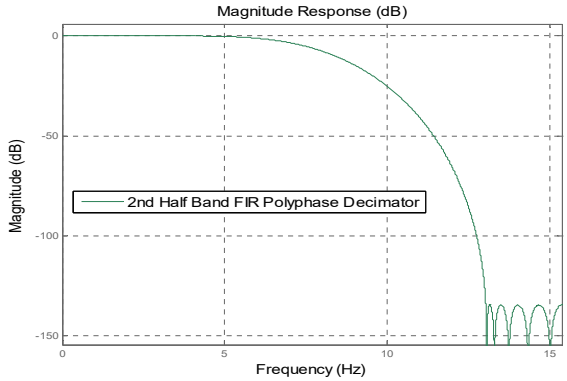

Figure 4. Second Stage Half Band Decimator Response

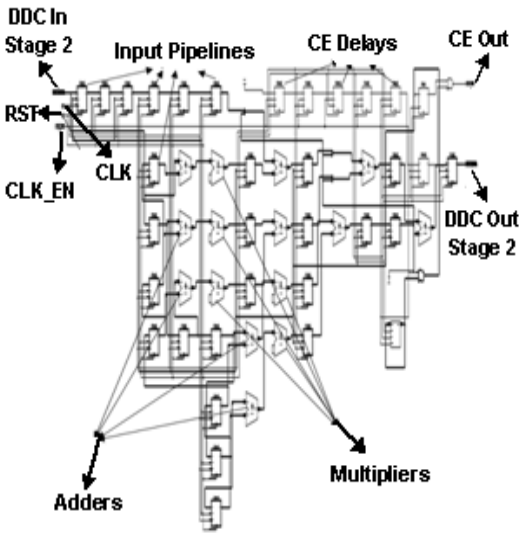

Figure 5. Stage 2 PSPMAC Based Decimator

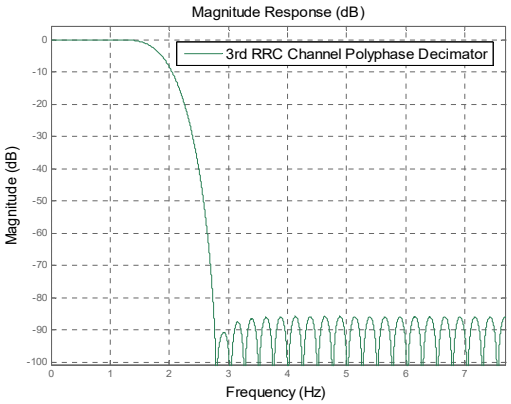

Figure 6. RRC Channel Filter

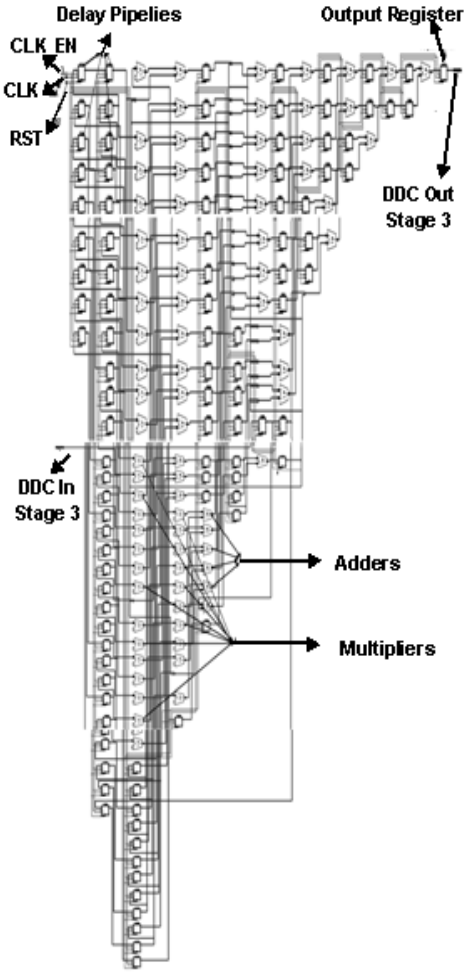

Figure 7. Stage 3 PSPMAC Based RRC Decimator

The second stage decimator requires 27 coefficients for its hardware implementation. To design the required decimator in PSPMAC style, 5 multipliers have been used as shown in Fig. 5. The input pipeline registers are used to store the new coefficient values required for processing in

the next cycle to enhance the speed further. The CE delays are used to make synchronization between stage 2 and stage 3. The next stage RRC filter is used for sampling rate conversion from 15.36 MSPS to 7.68 MSPS. This 2x over-sampling rate is needed in the timing recovery process to avoid the signal loss due to the sampling point misalignment. Root Raised Cosine (RRC) filter is designed with 1.92 MHz cut off frequency, 0.22 MHz roll-off factor and 50 dB side lobe attenuation using Chebyshev window [20] whose filter response is shown in Fig. 6. The third stage RRC decimator has also been designed using partially serial architecture as shown in Fig. 7.

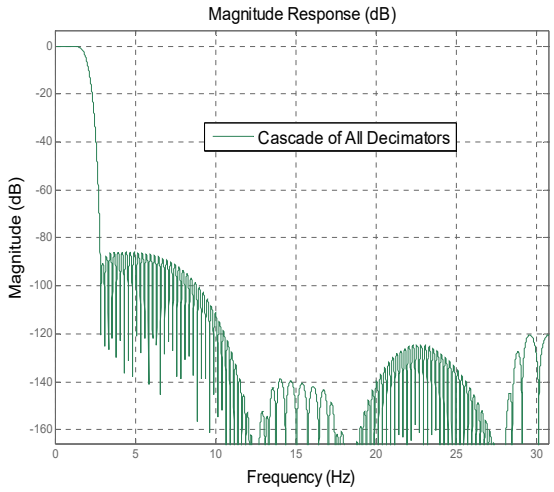

Figure 8. WCDMA DDC Output Response

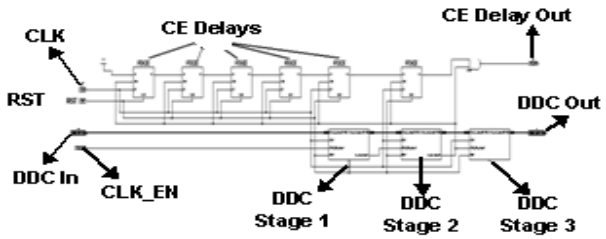

Figure 9. Proposed WCDMA DDC

The 61 coefficients required to design this RRC filter have been processed using 38 multipliers to improve both area and speed. The delay pipelining and output registers are used for synchronization. Finally, DDC is designed by cascading these three stages as shown in Figure 8 with 16 bit coefficients. The cascade of all optimized stages is shown in Fig. 9.

IV. H/W SYNTHESIS & SIMULATION

In the proposed DDC designs CORDIC algorithm based optimized DDS design is used in place of DDS compiler block to generate sinusoidal waveform needed for frequency translation [22]. The FIR Compiler blocks of existing designs are replaced by Equiripple techniques based decimators for optimal filter length to reduce the hardware requirement. It is further supported by the half band filter concept to improve the computational complexity for enhanced speed. Finally, the poly-phase decomposition technique is utilized in the hardware implementation of the proposed design to optimize both speed and area together by introducing the partially serial pipelined MAC architecture. The third stage of decimation has been developed using efficient RRC filter [23] design. All the decimators are implemented using MAC Algorithm with optimal number of embedded multipliers of target FPGA along with pipelined registers to enhance the speed performance and resource utilization. The Virtex-II Pro FPGA device is used for implementation that contains 136 embedded multipliers [24].

Two designs have been developed using different input output precisions. DDC is implemented using input precision of 14 bits and output precision of 16 bit and DDC 2 is implemented using input and output precision of 12 bits. The developed DDCs are simulated using Modelsim Simulator. The output response of DDC1 is shown in Fig. 10 and output response of DDC 2 is shown in Fig. 11. It can be observed from the simulated waveforms that the output response of both the designs is similar but speed performance of DDC2 is better as compared to DDC1.

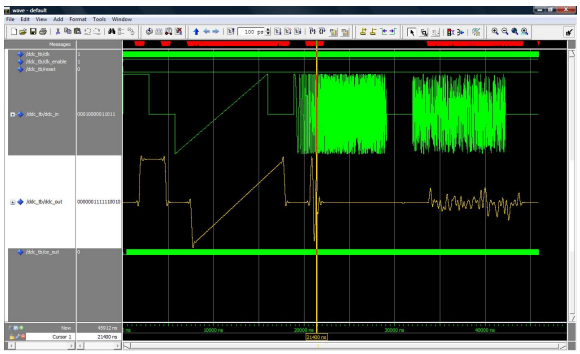

Figure 10. Optimized WCDMA DDC 1 Response

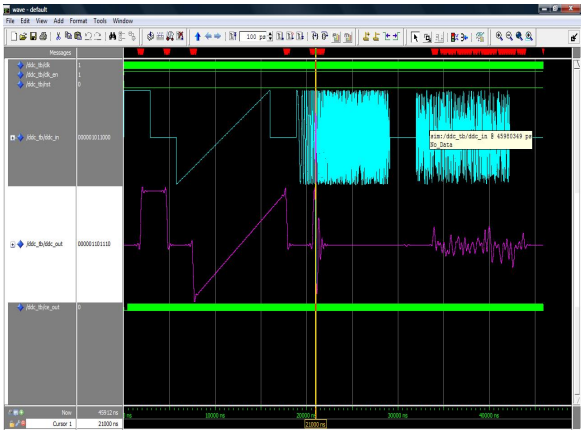

Figure 11. Optimized WCDMA DDC 2 Response

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The optimized DDC designs are finally mapped for hardware implementation and synthesised on Virtex-II Pro based xc2vp30-7ff896 target device. The resource consumption of the proposed design on specified target device is shown in Table I.

TABLE I. RESOURCE UTILIZATION

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Logic Utilization	DDC Design 1	DDC Design 2
Number of Slices	1477	1462
Number of Flip Flops	2535	2533
Number of LUTs	1429	1366
Number of I/Os	34	28
Number of MULT	46	46

The proposed optimized DDC 2 can operate at a maximum frequency of 146.36 MHz and DDC 1 can operate at 119 MHz as compared to 122.88 MHz in case of [20]. So the proposed DDC 2 provides an improvement of 19% in speed and DDC 1 provides almost the same speed as that of the existing DDC design. The developed DDC designs have shown better resource utilization as compared to DDC design of [21] which is shown in Table II.

TABLE II. RESOURCE UTILIZATION COMPARISON

Logic Utilization	DDC Design [21]	Proposed DDC Designs
Number of Flip Flops	4.93%	9%
Number of Slices	7.9%	10%
Number of MULT	3.8%	33%

V. CONCLUSION

This paper presents an efficient and cost effective DDC design for software defined radios. The existing DDC designs suffer from the drawback of cost effectiveness because their implementation includes DSP 48E slice based Virtex 4 and Virtex 5 FPGAs. The proposed DDC designs are developed and implemented on multiplier based Virtex II Pro target FPGA using optimized MAC algorithm. Three decimator stages are optimized separately and then cascaded together. The optimized DDC has been developed using partially serial pipelined MAC algorithm for area and speed optimization. The DDC designs are efficiently floor planned and routed to achieve the desired timing constraints. The developed DUCs have shown improved speed performance and resource utilization to provide cost effective solution for software radios.

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REFERENCES

[1] B. B. Carvalho, A. J. N. Batista, F. Patrício, M. Correia, H. Fernandes, J. Sousa, and C. A. F. Varandas, "Multi-Rate DSP/FPGA-Based Real-Time Acquisition and Control on the ISTTOK Tokamak" IEEE Transactions on Nuclear Science, VOL. 55, NO. 1, pp. 54-58, February 2008.

[2] Veerendra Bhargav Alluri, J. Robert Heath, Michael Lhamon "A New Multichannel, Coherent Amplitude Modulated, Time-Division Multiplexed, Software-Defined Radio Receiver Architecture, and Field-Programmable-Gate-Array Technology Implementation" IEEE Transactions on Signal Processing, Vol. 58, No. 10, pp. 5369-5384, October 2010.

[3] Amir Beygi, Ali Mohammadi, Adib Abrishamifar. "An FPGA-Based Irrational Decimator for Digital Receivers" IEEE International Symposium on Signal Processing and its Applications (ISSPA), pp. 1-4, 2007.

[4] Prashant Upadhyay, Rajesh Mehra, Nivedita Thakur "Low Power Design of an SRAM cell for Portable Devices", IEEE International conference on Computer and Communication Technology (ICCCT), pp.255-259, 2010.

[5] Takashi Shono, Yushi Shirato, Hiroyuki Shiba, Kazuhiro Uehara, Katsuhiko Araki, Masahiro Umehira, "IEEE 802.11 Wireless LAN Implemented on Software Defined Radio With Hybrid Programmable Architecture" IEEE Transactions on Wireless Communications, Vol. 4, No. 5, pp. 2299-2308, September 2005.

[6] Francois Rivet, Yann Deval, Jean-Baptiste Begueret, Dominique Dallet, Philippe Cathelin, Didier Belot, "A Disruptive Receiver Architecture Dedicated to Software-Defined Radio" IEEE Transaction on Circuits and Systems-II: Express Briefs, Vol.55, No. 4, pp. 344-348, April 2008.

[7] Pedro Cruz, Nuno Borges Carvalho, Kate A. Remley "Designing and Testing Software Defined Radios" IEEE Microwave magazine, pp. 83-94, June 2010.

[8] Navid Lashkarian, Ed Hemphill, Helen Tarn, Hemang Parekh, and Chris Dick "Reconfigurable Digital Front-End Hardware for Wireless Base-Station Transmitters: Analysis, Design and FPGA Implementation" IEEE Transactions on Circuits and Systems-I: Regular Papers, Vol. 54, No. 8, pp. 1666-1677, August 2007.

[9] Vandita Singh, Rajesh Mehra "Rational Rate Converter Design Analysis using Symmetric Technique", International Journal of Computer Trends and Technology, Vol. 27, No. 2, pp. 116-120, September 2015.

[10] G. Swathi, M. Revathy, "Design of a Multi-Standard DUC Based FIR Filter using VLSI Architecture", International Journal of Scientific Engineering and Research, Vol.3, Issue 11, pp. 41-44, November 2015.

[11] Renuka Verma, Rajesh Mehra, "FPGA Implementation of FIR Interpolator for IEEE 802.11n WLAN", International Journal of Engineering Science and Technology, Vol.8, Issue 7, pp. 121-127, July 2016.

[12] Renuka Verma, Rajesh Mehra, "Design of Low Pass FIR Interpolator for Wireless Communication Applications", International Journal of Advanced Research in Computer and Communication Engineering, Vol.6, Issue 7, pp. 355-362, July 2016.

[13] Fei Wang. "Digital Up and Down Converter in IEEE 802.16d", 8th international Conference on Signal Processing, pp. 16-20, 2006.

[14] Rajesh Mehra, Rashmi Arora "FPGA-Based Design of High-Speed CIC Decimator for Wireless Applications" International Journal of

 ISBN: 978-1-61208-506-7

Advanced Computer Science and Applications (IJACSA), USA, Vol. 2, No. 5, pp. 59-62, May-2011.

[15] Rajesh Mehra, Dr. Swapna Devi' "Efficient Hardware Co-Simulation of down Convertor for Wireless Communication Systems" International Journal of VLSI design & Communication Systems (VLSICS), pp. 13-21, Vol.1, No.2, AIRCC, June 2010.

[16] Xiaoxiao Xu, Xianzhong Xie, Fei Wang, "Digital Up and Down Converter in IEEE 802.16d" IEEE International Conference on Signal Processing (ICSP), Vol. 1, pp. 17-20, 2006.

[17] Saad Mahboob, "FPGA Implementation of Digital Up/Down Convertor for WCDMA System" IEEE International Conference on Advanced Communication Technologies (ICACT), pp. 757-760, 2010.

[18] Kong Chunli, Fan Xiangning, Xu Zhiyuan, Zheng Hao "Design and Simulation of Two-channel DDC in Satellite Cellular Integrated System" IEEE International Conference on Wireless Communication networking and Mobile Computing (WiCoM), pp. 1-4, 2010.

[19] Rajesh Mehra, "Reconfigurable Optimized WCDMA DDC for Software Defined Radios" Journal of Selected Areas in Telecommunications (JSAT), Cyber Journals: Multidisciplinary Journals in Science and Technology, Ontario, Canada, pp. 1-6, December Edition, 2010.

[20] Helen Tarn, Kevin Neilson, Ramon Uribe, David Hawke, "Designing Efficient Wireless Digital Up and Down Converters Leveraging CORE Generator and System Generator" Application Note on Virtex-5, Spartan-DSP FPGAs, XAPP1018 (v1.0), pp. 8-44, October 2007.

[21] LIN Fei-yu, QIAO Wei-ming, WANG Yan-yu, LIU Tai-lian, FAN Jin, ZHANG Jian-chuan, "Efficient WCDMA Digital Down Converter Design Using System Generator" IEEE International Conference on Space Science and Communication, pp. 89-92, 2009.

[22] Bindiya Kamboj, Rajesh Mehra "Efficient FPGA Implementation of Direct Digital Frequency Synthesizer for Software Radios" International Journal of Computer Applications, New York, USA, Volume 37, No.10, pp. 25-29, January 2012.

[23] Rajesh Mehra, Dr. Swapna Devi, "FPGA Implementation of High Speed Pulse Shaping Filter for SDR Applications" Springer International Conference on Recent Trends in Networks and Communications, Communication in Computer and Information Science (CCIS), Volume 90, Part 1, pp. 214-222, 2010.

[24] Xilinx User Guide "Virtex-II Pro and Virtex-II Pro X FPGA User Guide" UG012 (v4.2), pp. 178-185, November 2007.

 ISBN: 978-1-61208-506-7