FEM Modeling for PCB Assembly Simulation

Ming-Hsiao Lee, Jiunn-Horng Lee, Chih-Min Yao, Jen-Gaw Lee
National Center for High-performance Computing, NARL
30076 Hsinchu City, Taiwan
Email: {9303103, jhlee, 9403116, jglee}@narlabs.org.tw

***Abstract*— A Printed Circuit Board (PCB) is a multi-layered composite, which consists of several layers of copper circuits and dielectric materials. It is used as a backbone to carry and connect various electronic components, i.e., PCB Assembly (PCBA), to achieve certain functions. Currently, most of the products need PCBAs to fulfill their functions. Nevertheless, because the components, e.g., chips, are decreasing in size, the accuracy and reliability of PCBAs have become critical issues, either in manufacturing processes or in actual uses. One of the serious problems is the warpage of the PCB, which is induced by the thermal mismatch due to unevenly distributed circuits and multi-materialled components during the manufacturing process, which experiences a large temperature change. This may cause defects and failures in the assemblies, e.g., the chips and PCB are not well connected due to the dislocation. It is helpful to simulate in advance to evaluate possible defects. However, since the circuits on a PCB are very tiny, compared with the size of the PCB or the components, it is unpractical and not feasible to build a Finite Element Method (FEM) model to include all the details of circuits and components, which are attached to the PCB with a big amount of solder joints. To avoid the difficulties, a new effective modeling approach, which adopts equivalent material properties, is proposed for PCBA's simulation. In this approach, the multi-layered PCB and the attached components are modeled with a moderate mesh, while the circuit's and solder joint's effects are still included. With the proposed approach, the analysis model can be useful and efficient for simulating the PCBA to evaluate the manufacturing process and structural characteristics of the PCBA.**

Keywords- PCB; PCBA; Warpage; Trace mapping.

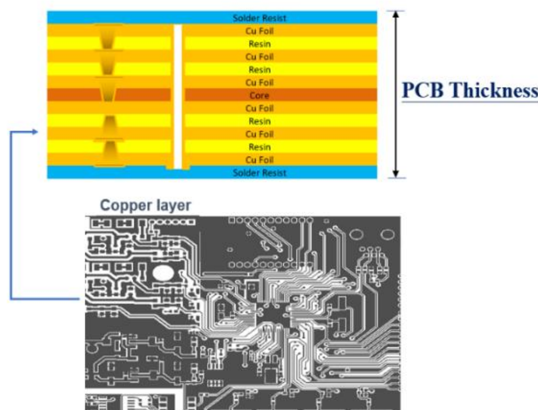

Figure 1. A typical stack-up of a PCB.

I. INTRODUCTION

A PCB is a multi-layered composite, which includes many layers of copper circuits and dielectric materials, as shown in Figure 1. Currently, the circuit trace width on the board is getting smaller. Due to the unevenly distribution of the circuits on different copper layers, the layer's stiffnesses, and thermal expansion coefficients are also unevenly distributed, which affect the characteristics of the board's structural behaviors, especially causing warpage due to thermal mismatch. Therefore, to evaluate the design, the distribution of circuits should be taken into account during the structural analyses. Nevertheless, the trace width and thickness are so tiny, i.e., in the order of microns or sub-microns, much smaller than that of the PCB board, i.e., normally in the order of centimeters. Moreover, one PCB may consist of tens of trace layers and dielectric layers. If all the traces are also meshed, the element size could be extremely small, i.e., in the order of microns or sub-microns, and then the whole model could reach billions of elements. This is not a workable case. This type of case actually is a multi-scaled problem. To simulate this type of problem, often an equivalent material approach [1] is adopted. Here, as proposed, first, the multi-layered PCB structure is meshed independently of the circuits so that the mesh size is not affected by the width of the traces. Instead, a moderate element size can be chosen. Then, the circuit part adopts an equivalent material approach; it is to calculate the area ratio of copper circuits distributed on each element of the circuit layers, so called trace mapping, as shown in Figure 2.

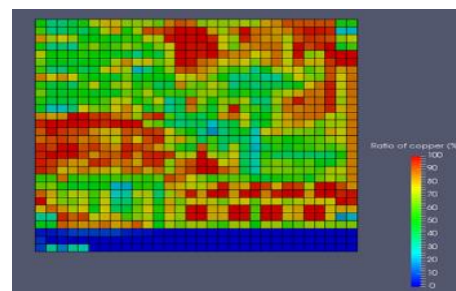

Figure 2. Copper (trace) ratio distribution.

Courtesy of IARIA Board and IARIA Press. Original source: ThinkMind Digital Library https://www.thinkmind.org

Copyright (c) IARIA, 2024. ISBN: 978-1-68558-184-8

After the copper ratio on each element of the circuit layer is obtained, calculate its equivalent material properties, such as Young's modulus and the coefficient of thermal expansion, according to the copper ratio [2][3][4] (Zwemer et al. and Bajaj et al. tackle only the PCB with the equivalent material property approach). More than that, the relationship between the equivalent material properties and the copper ratio can be also derived by a numerical test measure, as the one shown in Figure 3. It is like tensile testing, i.e., test models with various copper ratios are analyzed to inversely derive their equivalent material properties, such as Young's modulus. Then, the relationship between the Young's modulus and the copper ratio is obtained and used to calculate the equivalent material properties for each circuit layer element. Once the generated FEM models including equivalent material properties for each element on different trace layers are ready (all are generated automatically with the self-developed programs), the FEM model can be solved with available solvers, e.g., Calculix (an open-source software) [5]. With this approach, although the circuit layer effect has been included, the mesh model is still moderate and suitable for the analysis. Similarly, PCB with mounted chips (PCBA) can be simulated in the same way. However, the chips and the solder bump layers, which mount the chips onto the PCB, also need to take advantage of equivalent material approach in order to solve the cases efficiently.

The rest of the paper is structured as follows. In Section II, we present the simulation processes and results. We finish in Section III with some concluding remarks.

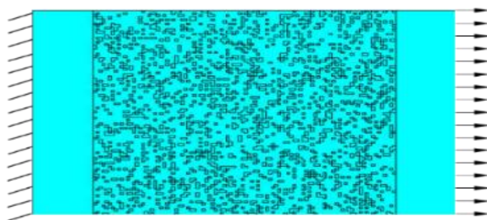

Figure 3. Calculation setting for equivalent material proprieties.

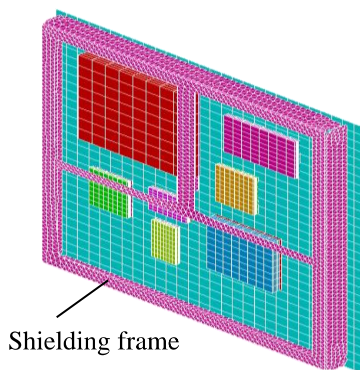

Figure 4. A typical PCBA with shielding frame.

II. RESULTS

A PCBA, as shown in Figure 4, usually is manufactured in batches; each batch includes several pieces of the final PCBA modules, as shown in Figure 5. The warpage could happen during the manufacturing processes, e.g., the Surface Mount Technology (SMT) process, which experiences a great temperature change. This is mainly induced by the thermal mismatch due to the unevenly distribution of circuits, multi-materialled chips, the shielding frames, etc. Figure 5 shows warpage of a batch panel of PCBAs. If the warpage is large, it may cause defects and failures in the assemblies, e.g., the chips and PCB are not well connected due to the dislocation. In addition, in many circumstances during the use, the cyclic temperature change, as a cyclic loading, could also cause fatigue failures. This is also a typical problem for the PCBA.

The structure of a PCBA is not only extremely complicated, but also multi-scaled, so simulating the PCBA has been a challenging problem. However, the proposed effective modeling approaches for the tiny circuits and solder joints can effectively solve these difficulties. It can distinctly reduce the size of the analysis model and efficiently handle the effect of the circuits and solder joints for the simulation. With the effective modeling approaches, evaluating the structural behaviors of PCBAs becomes simple and efficient. Moreover, even irregular-shaped PCBs can be handled, as shown in Figure 6.

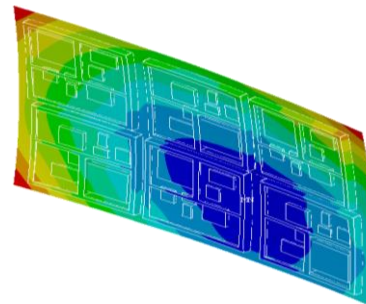

Figure 5. Warpage of a PCBA panel.

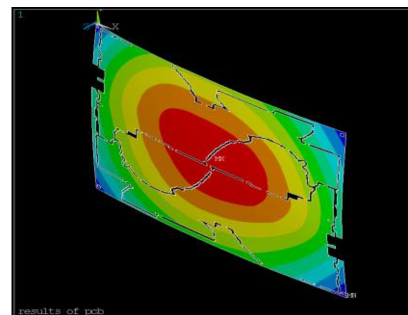

Figure 6. Warpage of an irregular-shaped PCB.

Courtesy of IARIA Board and IARIA Press. Original source: ThinkMind Digital Library https://www.thinkmind.org

Copyright (c) IARIA, 2024. ISBN: 978-1-68558-184-8

To verify the adopted approaches, a real test case was conducted, as shown in Figure 7. A typical PCBA case was conducted to go through a standard manufacturing process, i.e. a temperature change. Although the PCBA module (60 mm x 60 mm) includes many chips, for the simulation, only four main chips, i.e., one CPU (Central Processing Unit), two DRAMs (Dynamic Random-Access Memory), one PMIC (Power Management IC), are included. Other components or chips are very small and ignored. This PCB consists of, totally, 21 layers, including 10 trace layers. The equivalent material properties, e.g., Young's modulus, of each element on each trace layer are calculated according to the derived copper ratio. With all these data and model, the analysis was conducted. The comparison of the maximum warpage (out-of-plane displacement) between the simulation and experiment is shown in Table 1. It shows the difference is around 17%. For such a complicated case, this can validate the proposed approaches.

TABLE 1. MAXIMUM WARPAGE COMPARISON

	Simulation (µm)	**Experiment (µm)**
Maximum Warpage	169	140

In addition, a PCBA case with shielding frames was also conducted. The analyses have found some warpages seriously affected by shielding frames, as shown in Figures 4 and 5. Although the original purpose of the Electromagnetic Compatibility (EMC) shielding frame is to prevent Electromagnetic Interference (EMI) or Radio Frequency Interference (RFI), not for structural considerations; however, they cause some side effects. This finding also shows that the proposed approaches can be useful for the evaluation and design.

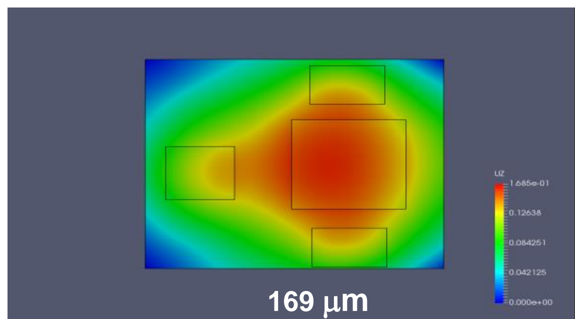

Figure 7. Warpage of a tested PCBA.

III. CONCLUSION

The structure of a PCBA is not only extremely complicated, but also multi-scaled, so simulating the PCBA has been a challenging problem. However, the proposed effective modeling approaches for the tiny circuits and solder joints can effectively solve these difficulties. It can distinctly reduce the size of the analysis model and efficiently handle the effects of the circuits and solder joints for the simulation. With the effective modeling approaches, evaluating the structural behaviors of PCBAs becomes simple and efficient. The test case shown above proves the effectiveness of the approaches. In addition, the fact that the warpage is affected seriously by the shielding frame has been found, although the original purpose of the shielding frame is not for structural considerations. This finding also demonstrates that the proposed approaches can be helpful. Nevertheless, because a PCBA consists of many chips, which may come from different vendors, the data of the internal structures and used materials of the chips may not be sufficient. In this situation, the accuracy of the results would be affected.

REFERENCES

[1] H. C. Cheng, K. N. Chiang, and M. H. Lee, "An Effective Approach for Three-Dimensional Finite Element Analysis of Ball Grid Array Typed Packages," Journal of Electronic Packaging, ASME, vol. 120, pp. 129-134, 1998.

[2] D. Zwemer et al., "PWB Warpage Analysis and Verification using an AP210 Standards-Based Engineering Framework and Shadow Moir," EuroSimE 2004, Brussels, Belgium, pp. 121-131, May 10-12, 2004.

[3] M. Bajaj et al., "Automating Thermo-Mechanical Warpage Estimation of PCBs/PCAs Using a Design-Analysis Integration Framework," Mentor U2U, San Jose, CA, USA, May 3-5, 2006. Available from: https://tsapps.nist.gov/publication/get_pdf.cfm?pub_id=32287

[4] D. H. Kim, S. J. Joo, D. O. Kwak and H. S. Kim, "Warpage Simulation of a Multilayer Printed Circuit Board and Microelectronic Package Using the Anisotropic Viscoelastic Shell Modelling Technique That Considers the Initial Warpage," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 6, no. 11, pp.1667-1676, 2016.

[5] Calculix: https://www.dhondt.de/. [accessed Sept. 2024]

Courtesy of IARIA Board and IARIA Press. Original source: ThinkMind Digital Library https://www.thinkmind.org

Copyright (c) IARIA, 2024. ISBN: 978-1-68558-184-8