Design and Analysis of a Dual Loop CDR using Maneatis Delay Cell VCO

Khalil Ibrahim Mahmoud, J. Dhurga Devi, and P.V. Ramakrishna
Department of Electronics and Communication Engineering
College of Engineering, Anna University, Chennai, INDIA 600025
khalilaljabory@gmail.com, j_dhurgadevi@annauniv.edu, pvramakrishna@annauniv.edu

Abstract — **Clock and Data Recovery (CDR) circuits have been used extensively in the receivers of optical communication systems, and a variety of applications of inter and intra chip communications. The primary design/performance metrics of CDR circuits are clock jitter, lock range, acquisition time, power consumption, silicon area, and noise immunity. The main source of jitter is the power supply noise. The present paper investigates the effects of power supply noise on the jitter performance of the well known dual loop architecture of CDR system. In order to improve the jitter performance of the dual loop CDR system, the VCO alone is replaced by the self-biased Maneatis VCO which is well known for its immunity to power supply noise and process variations. The Maneatis VCO is widely used for microprocessors PLL systems but it is rarely used in CDR systems. The combination of the dual loop architecture and self-biased Maneatis VCO together provides the benefits of both schemes.**

Simulations were then carried out systematically to determine the capability of the proposed CDR circuit to tolerate power supply noise. The results presented in this paper show that while the conventional dual loop architecture cannot tolerate more than 20mV@10MHz noise on power supply terminal, the proposed CDR architecture can tolerate up to 200mV@10MHz noise on the power supply without degradations in jitter performance.

Keywords- CDR, PLL, VCO, Jitter, Power Supply Noise.

I. INTRODUCTION

During the past few decades, the CDR circuits have played an important role in a wide range of applications such as Gigabit Passive Optical Network (GPON), Gigabit Ethernet Passive Optical Network (GEPON), Synchronous Optical Network (SONET), optical transmission receiver, chip-chip interconnections, DDR, System on Chip (SOC), serial link communications, and PCI. The CDR circuits are normally used to extract the clock embedded in the received data and used to re-time and re-sample the received (distorted) data for further synchronous processing.

The most important metric of CDR system performance is the jitter on the recovered clock, and it represents the deviations of the clock transitions from the ideal one. The state of the art CDR circuit architectures, and the trade-offs and techniques for reducing the jitter are discussed in recent tutorials [3]-[6]. Of late, with the increased integration of analog and digital functions on the same chip, immunity to power supply noise has emerged as a very important design constraint. Several studies on the mitigation of power supply noise on PLLs have been reported in [7]-[10]. In addition to using differential topologies, some of these studies suggest the use of regulators as common techniques used to mitigate the power supply noise. The design of PLLs considering immunity to power supply noise as a design constraint is presented in [9] and considers variants of the Maneatis VCO [11, 12] in the context of PLLs and their sensitivities to power supply noise. A fast Matlab simulation procedure for evaluating the impact of power supply noise on CDR system has been described in [10].

Very few studies on the mitigation of power supply noise for CDRs have been reported in the literature. The present work addresses this particular aspect of CDR circuits, specifically in the context of dual loop delay interpolating architectures. Although there are many architectural choices, the dual loop delay interpolating CDR described in [1]-[3] is chosen for the present study since this is considered as one of the important architectures for realizing CDR circuits with a wide operating frequency range while at the same time providing low jitter.

The symmetric load, self-biased Maneatis VCO proposed by [11, 12], is well known for its ability to mitigate power supply noise and for this reason and is widely used in many of the state of the art of microprocessor PLLs. The present study investigates the possibilities of using this VCO in CDR circuits. It was observed that the Maneatis VCO as proposed in [11, 12] could not be used as such in the original dual loop CDR architecture since the former had only one control voltage input while the latter required a VCO with a coarse as well as fine control voltage inputs. Hence, in the present study, the bias generator of the self-biased Maneatis VCO from [11, 12] was suitably modified and then was incorporated into the CDR circuit. It is demonstrated in this paper that the modified Maneatis VCO is capable of providing improved performance with respect to power supply noise. Specifically, simulation results show that the proposed scheme tolerates up to seven times the power supply noise than in the conventional dual loop CDR for similar jitter performance.

The present paper is organized as follows. Section 2 presents a brief description and design details of the well-known dual loop delay interpolation CDR. Section 3 discusses the proposed modification of the Maneatis VCO for incorporation into the dual loop CDR design. Section 4 gives the simulation results of noise performance for the delay interpolation dual loop CDR as well as for the proposed modified Maneatis dual loop CDR and in Section 5, the conclusions are presented.

II. THE DUAL LOOP CDR SYSTEM DESIGN

The block diagram of the dual loop delay interpolating CDR is shown in Fig. 1 and is the same as the one presented in [1, 2]. This system will be considered as a reference system against which the performance of the proposed modifications will be compared. The system shown in Fig. 1 consists of a coarse FLL and a fine PLL which operate together on the input data sequence and recover the clock which could be subsequently used for retiming the data.
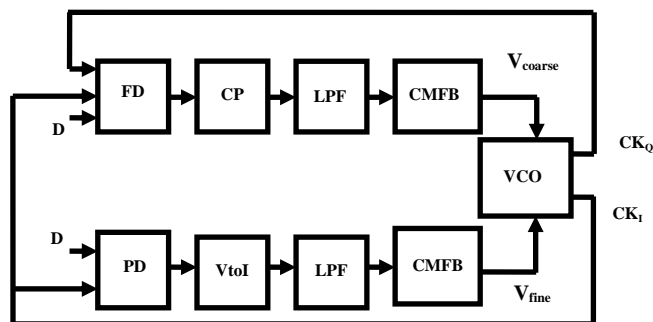

Figure 1. The Complete CDR System Block Diagram

The FLL provides a coarse acquisition of the clock and operates over a wide frequency range. It comprises of the Frequency Detector (FD), the Charge Pump (CP), the Low Pass Filter (LPF), Common Mode Feedback (CMFB), and a delay interpolating VCO. The FD is realized using a digital quadricorrelator and detects the frequency difference between the input data rate and the internally generated clock by the VCO. The outputs of the FD are the "UP" and "DOWN" pulses that have constant pulse durations and the number of pulses generated in a given time interval depends on the frequency difference. These pulses are fed to the charge pump, where they are converted into proportional charging and discharging currents for the LPF. The details of circuit design for individual blocks of the FD are given in [1, 2] and the same procedure has been adopted for the present work.

The design equations given below are from [1, 2, 13] and are used to determine the LPF parameters of the FLL.

$$\omega_c = \frac{I_{cp}.K_{VCO}.k_p}{2.\pi} \tag{1}$$

$$\omega_z = \frac{\omega_c}{5} = \frac{1}{R_p.C_p} \tag{2}$$

$$\omega_p = 5.\omega_c = \frac{C_p + C_s}{C_p.C_s.R_p} \tag{3}$$

$$C_s = \left[\omega_p.R_p - \frac{1}{C_p} \right]^{-1} \tag{4}$$

The symbols ω_c, ω_z, ω_p, ζ, and K_{VCO} in the above equations represent the crossover frequency, pole frequency,

zero frequency, damping ratio, and VCO gain, respectively. The symbols R_p, C_p, and C_s represent the shunt resistor, capacitor and parallel smoothing capacitor, respectively.

The PLL in Fig. 1 has a much smaller capture range and operates after the FLL has acquired lock and this combination of FLL lock followed by PLL lock reduces the jitter in the recovered clock considerably. The PLL loop consists of a Phase Detector (PD), a Voltage-to-Current converter (V/I), and the LPF. The PD is an analog sample and holds system which consists of a two sample and hold circuits and a multiplexer. The output of the PD is a differential voltage proportional to the input phase difference. These voltages are converted to proportional currents by the V/I converter and are used as the charging and discharging currents of the LPF of the PLL block.

The VCO is a ring oscillator which is common to both FLL and PLL is realized with four delay cells and uses the delay interpolation concept with two paths, the fast path and the slow path. Fig. 2 shows the delay interpolation concept realized in the delay cell. The fast path consists of a differential stage, while the slow path consists of a constant delay stage and a differential stage. The two paths share the same output load. The output current is the sum of the slow and fast currents and is constant. The slow and fast currents are steered differentially depending on the control voltages to maintain constant sum.
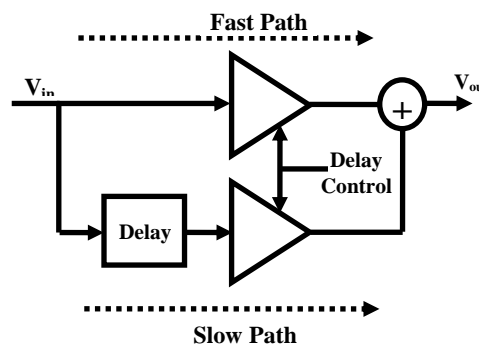

Figure 2. Shows the Delay Interpolation Concept

As in the case of the LPF of the FLL, the design procedure for determining the PLL loop filter parameters are adopted from [1, 2, 13] and the design equations are listed below:

$$\tau_2 = \frac{2.\zeta}{\omega_n} \tag{5}$$

$$K = K_{pd}.K_{VCO}.\frac{\pi}{4} \tag{6}$$

$$K = 2.\zeta.\omega_n.\sqrt{\frac{\tau_1}{\tau_2} + 1} \tag{7}$$

$$\tau_1 = \left(R_{f1} + R_{f2} \right) C \tag{8}$$

$$\tau_2 = R_{f2}.C \qquad (9)$$

Where the symbols τ_1, τ_2, R_{f1}, R_{f2}, and c are represent the time constants, series resistor, shunt resistor and capacitor, respectively, of LPF of the PLL. The symbols ω_n, ζ, K, K_{PD}, K_{VCO} are the natural frequency, damping ratio, open loop gain, phase detector gain, and VCO gain, respectively and these values can all be determined once the operating frequency, bias currents and technology node of the CMOS process are chosen.

Detailed simulations have been carried to determine the performance of the dual loop delay interpolation CDR with respect to power supply noise. Though the details and quantitative results of these simulations are presented subsequently in Section 4, the conclusion that clearly emerged from these simulations was that the performance of the dual loop delay interpolation CDR was very sensitive to power supply noise, and that one cannot possibly use this CDR without dedicated regulators providing clean power supply to the whole system.

III. THE MANEATIS DELAY CELL-BASED VCO AND ITS MODIFICATION

It is well known from the PLL literature that the major contribution to jitter (or phase noise) due to power supply noise comes from the VCO block of the PLL, and this was true in the present CDR case as well (quantitative results given in the next section). Since the Maneatis Delay Cell-based VCO is well known for its immunity to power supply noise, the adaptation of this VCO to the dual loop CDR is described next.

The block diagram of the original Maneatis VCO and its associated bias generator are shown in Fig. 3 and Fig. 4, respectively. The Maneatis VCO shown in Fig. 3 basically comprises of four symmetric load delay cells for which the control voltages come from the bias generator circuit in Fig. 4. The Maneatis Delay cell-based VCO posses two salient features, first is its high supply immunity, and the second is its symmetric load resistance based delay element. The latter enables the VCO to have a wide operating frequency range. The symmetric load resistance can also reject the supply noise (dynamic supply noise rejection) and is obtained by having the lower limit of the voltage swing to be equal to the control voltage itself. Further, for static supply noise rejection, it is required that $V_{control}$ track the supply voltage variations and hence it is referenced to (V_{DD}) in [11, 12]. From this $V_{control}$, one has to generate two bias voltages V_{bp} and V_{bn} to be fed to the VCO of Fig. 3. Of these, V_{bp} tracks the supply voltage changes to keep the load resistance of the delay cell and hence, the output frequency constant. On the other hand, V_{bn} is kept independent of supply voltage changes in order to keep the tail current constant. It can be seen that the conventional bias generator shown in Fig. 4 can accept only one control voltage $V_{control}$, and hence cannot be directly incorporated directly into the dual loop CDR of Fig. 1.

To provide an option for accepting coarse and fine control voltages, the bias generator of the Maneatis VCO has been modified and is shown in Fig. 5. In this modified circuit, the coarse and fine control voltages are provided as gate voltages to two NMOS transistors which act as voltage controlled current sources (tail sources). These currents are summed up to form the drain current of a single PMOS transistor. Since the source of this diode connected PMOS transistor is connected directly to the supply rail, its gate voltage tracks the changes in supply voltage while maintaining the current set by the bottom tail transistors. This gate voltage of the PMOS is then used as part of a feedback loop containing the half replica delay cell to generate the bias voltages V_{bp} and V_{bn} which are used finally by the delay elements of the VCO. The final block diagram of modified Maneatis delay cell VCO is shown in Fig. 6. The voltage, V_{bp}, produced by the bias generator tracks the supply voltage and sets the lower limit of the oscillation swing (and the load resistance) to fix the output frequency. On the other hand, since the course ($V_{bn-coarse}$) and fine control voltages ($V_{bn-fine}$) are referenced to the ground terminal, the final voltage V_{bn}, which determines the tail current in the delay element, keeps the tail current constant.
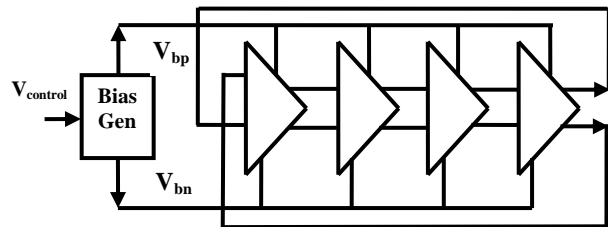

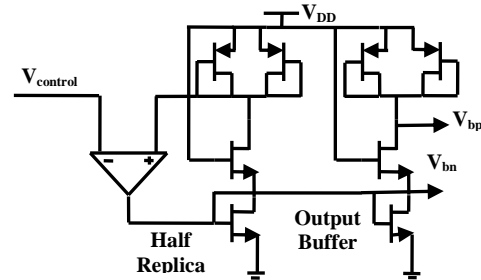Figure 3. The original Maneatis VCO

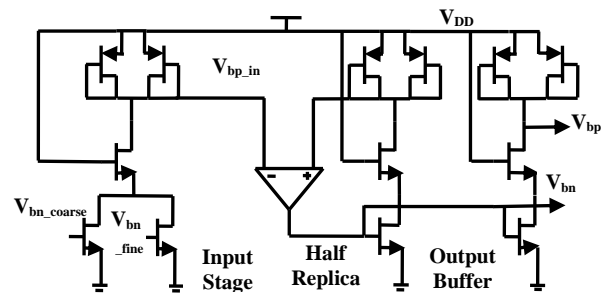Figure 4. Original Bias Generator
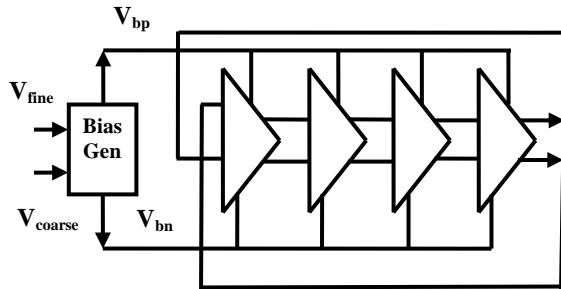

Figure 5. Modified Bias Generator

Figure 6.   The proposed modified VCO

The simple modification proposed above for the bias generator provides a method for combining the coarse and fine control voltages while retaining the robustness of the original Maneatis VCO. The sensitivity of this VCO to power supply voltage variations were first assessed and then the VCO was incorporated into the original dual loop CDR scheme of Fig. 1. Using the same system specifications and design equations described earlier in Section 2, the parameters of the LPFs for the FLL and PLL have been determined and are listed in Table I. These parameters are different from those of the delay interpolation VCO because the coarse and fine gains of the modified Maneatis VCO are different from that of delay interpolation VCO.

IV.   SIMULATION RESULTS AND DISCUSSION

In this section, first, quantitative results related to the supply noise performance of the delay interpolating VCO based CDR are presented. Next, simulations results are presented to validate the modification carried out on the Maneatis VCO and also to demonstrate that it can indeed replace the delay interpolation VCO in the original dual loop CDR. Finally, for the modified dual loop CDR, simulation results related to its performance with respect to power supply noise are presented.

All simulations have been carried out using the Cadence Spectre tool. The devices chosen for the simulations are from the 0.35μm CMOS technology libraries from Austriamicrosystems and the various over-drive voltages and bias currents are chosen accordingly. For the present work, a nominal data rate of 833 Mbps is chosen for the CDR, the FLL cross over frequency is chosen as 30MHz, and the charge pump current of the FLL is found to be 125μA. The PLL loop natural frequency ω_n, and damping ratio ζ are chosen to be 0.5 MHz and 4, respectively. The FLL and PLL LPF parameters have been determined for the above system specifications and given in Table I. For clock recovery simulations, PRBS data of length 2^{14} were used as input data to the CDR system.

First, the delay interpolation VCO characteristics are given in Fig. 7 where the output frequency dependence on coarse and fine control voltages is shown. The coarse and fine gains are found to be 506MHz/V and 65.9MHz/V, respectively. Similarly, the modified Maneatis VCO circuit was simulated and Fig. 8 shows the corresponding VCO gains plots. The coarse and fine gains were found to be 3GHz/V and 230MHz/V, respectively.
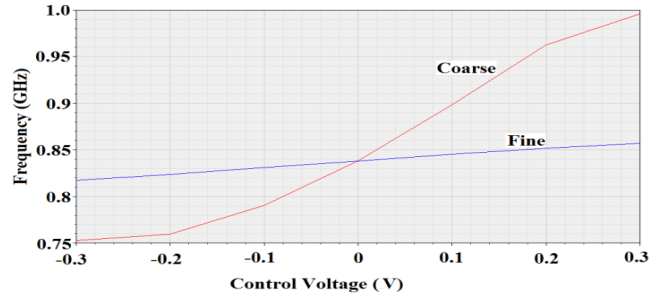

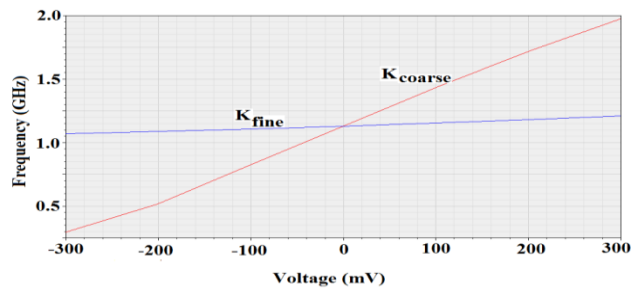Figure 7.   Coarse and Fine Gains of the Delay Interpolation VCO

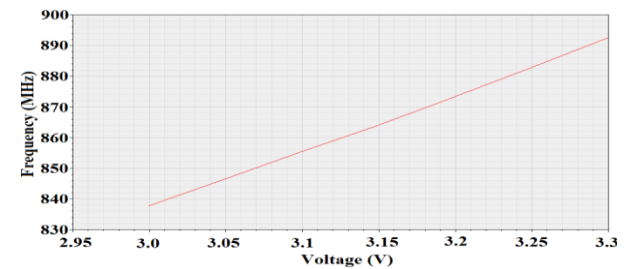Figure 8.   Coarse and Fine Gains of the Modified Maneatis VCO

Figure 9.   The Delay Interpolation VCO Sensitivity to Power Supply Noise

The static supply sensitivity of the delay interpolation VCO is shown in Fig. 9. For a nominal control voltage (Vc=0.74V, Vf=0.74V), it is found to be 185MHz/V and represents 6.6% frequency change for 10% change in the supply. The corresponding static supply sensitivity of the modified Maneatis VCO is shown Fig. 10.
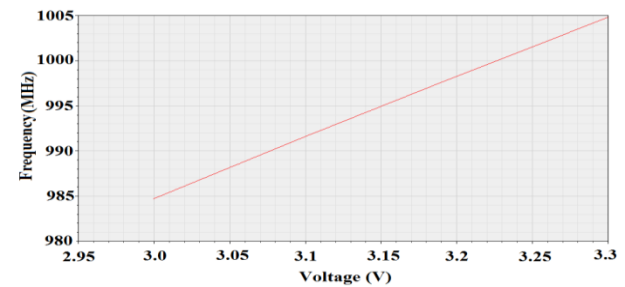

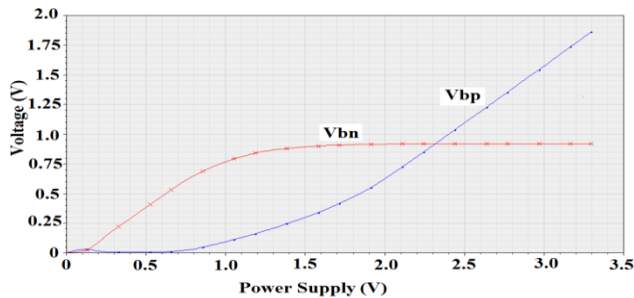Figure 10. The Modified Maneatis VCO Sensitivity to Power Supply Noise

Figure 11. Variations of Vbn and Vbp versus Power Supply Voltage

For a nominal control voltage (Vc=0.95V, Vf=1.05V), it is found to be 67MHz/V and represents 2.4% frequency change for 10% power supply change. The reduction in sensitivity of the modified Maneatis VCO is to be expected and is due to the ability of the bias generator to track the variations of the power supply voltage and is demonstrated in Fig. 11. The variations of V_{bn} and V_{bp} with respect to V_{DD} are plotted in Fig. 11 while maintaining the coarse and fine voltages constant and it can be seen V_{bn} is independent of V_{DD} while V_{bp} tracks V_{DD} for static power supply variations. Incidentally, the modified Maneatis VCO also has better power supply sensitivity of 67MHz/V as compared to the value 158MHz/V reported recently in [14], though the latter is for a PLL and for a somewhat higher frequency.

Next, with PRBS data input, clock recovery was carried using two the CDR schemes using clean power supplies. The capture transient showing the evolution of coarse and fine control voltages of the dual loop delay interpolation CDR and the dual loop modified Maneatis CDR are depicted in Fig. 12 and Fig. 13, respectively. For the dual loop delay interpolation CDR, the lock time, the steady state ripple on the fine control voltage, and the recovered clock jitter are 1μsec, 50mV and 4.3psec (0.4%UI), respectively. The corresponding quantities are for the dual loop modified Maneatis CDR are 0.6 μsec, 10mV, and 8.4 psec (0.7%UI), respectively.
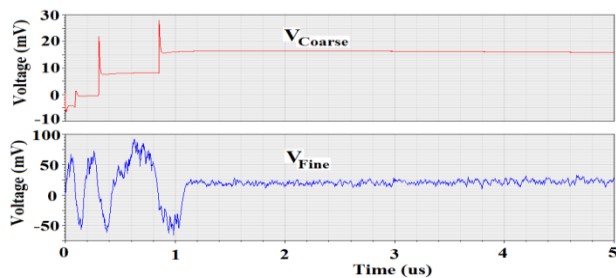

Figure 12. CDR Coarse and Fine Control Voltages with Clean Power Supply for Delay Interpolation VCO
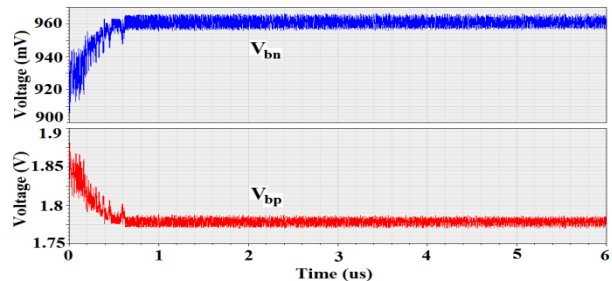

Figure 13. CDR Control Voltages with Clean Power Supply for Modified Maneatis VCO

Immunity of the two CDR schemes to power supply noise is characterized by adopting the procedure followed in [11, 12]. Noise sources in the form of sinusoidal signals of different frequencies and amplitudes were superposed on the VDD supply node. The effects of this noise source on the CDR system are measured by two ways. First by measuring the ripple on the differential fine control voltage and the second one is measuring the rms jitter on the recovered clock.

Table II provides the jitter performance of the dual loop delay interpolation CDR with noise injected individually into the power supply node of the different blocks of the CDR. Each column of the table indicates the ripple on the control voltage (after lock) of the dual loop CDR and the jitter on the recovered clock for a specific noise amplitude. It can be seen that the VCO is the most sensitive block and causes maximum degradation of performance. It was also found that the system fails to lock if the noise amplitude is increased beyond 30mV. Fig. 14 shows the differential fine control voltages of the dual loop delay interpolation CDR with noise of 20mV@10MHz on power supply terminal. For comparison, the same parameters are plotted for the dual loop modified Maneatis CDR in Fig. 15 but with a power supply noise of 200mV@10MHz.
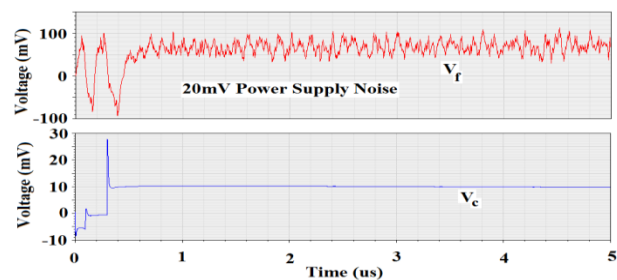

Figure 14. CDR Control Voltages with 20mV@10MHz Power Supply Noise for Delay Interpolation VCO
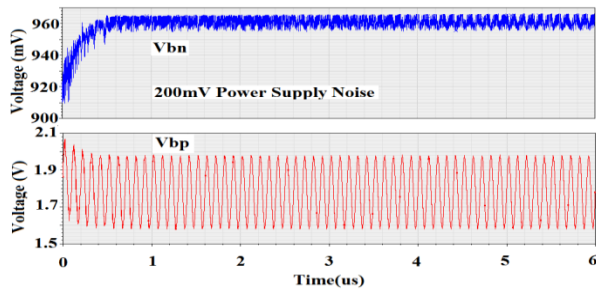
Figure 15. CDR Control Voltages with 200mV@10MHz Power Supply Noise for Modified Maneatis VCO

Finally the jitter performance of the integrated dual loop delay interpolation CDR and the proposed dual loop modified Maneatis CDR are given in Table III. It can be seen that the performance of the latter with 200mv noise is comparable to that of the former with a 30 mV noise on the supply line. The ripple voltage on the control voltage is not listed for the proposed CDR since this tracks the noise on the supply voltage as it is supposed to.

Since the Maneatis VCO and the delay interpolation VCO of the original dual loop scheme are both differential delay cell-based ring oscillators, their power consumption is nearly the same. Since the loop parameters for the proposed scheme have been chosen to be the same as that of the original dual loop scheme, the acquisition time is also nearly the same. Maneatis VCO is inherently known to have a wide range of operating frequencies.

V. CONCLUSIONS

While it is noted in the literature that the dual loop CDR architecture has certain important desirable features not available in other architectures (see [15] for example), there are no studies reporting its jitter performance with respect to power supply noise. While this might not have been an issue in the older technologies where dedicated external regulators providing clean supplies to the CDR can be assumed, in the context increased integration and System on Chip (SOC) schemes, on chip power supply noise often becomes a serious issue. The results presented in this paper provide three important conclusions. The first is that the original dual loop CDR as proposed in [1] is very sensitive to power supply noise and may require dedicated power supply regulators. The second conclusion is that the original Maneatis delay VCO can indeed be easily modified for incorporation into the dual loop CDR. The third conclusion is that the resulting modified dual loop CDR is capable tolerating nearly 200 mV noise on the supply line without degradation in performance. This in turn indicates that it can be easily integrated onto (SOC) architectures without requiring dedicated supply regulators.

TABLE I. THE PLL AND FLL LPF PARAMETERS

CDR in Ref. [5]				CDR with proposed VCO			
PLL		*FLL*		*PLL*		*FLL*	
R1 (kΩ)	996	*Rp (kΩ)*	3	*R1 (MΩ)*	4	*Rp (Ω)*	503
R2 (kΩ)	107	*Cp (pF)*	9	*R2 (kΩ)*	107	*Cp (pF)*	53
C (pF)	150	*Cs (fF)*	371	*C (pF)*	150	*Cs (pF)*	2

TABLE II. JITTER ON RECOVERED CLOCK OF THE CDR WITH VCO OF REF. [5]

Parameters	with Noisy Power Supply		
Noise amplitude at 10MHz (mV)	10	20	30
Jitter on Recovered clock ps, (%UI)	25, (2)	52, (4)	63, (5)
Ripple on Vfine (mV)	50	55	60

TABLE III. BLOCKWISE NOISE PERFORMANCE OF THE CDR WITH VCO OF REF. [5]

Parameters	With Noisy Power Supply Only On				
Noise of 20mV at 10MHz	VCO	FD	PD	CP	VtoI
Jitter on Recovered clock ps, (%UI)	50, (4)	11, (1)	11, (1)	8, (1)	16, (1)
Ripple on Vfine (mV)	75	50	45	50	40

TABLE IV. JITTER ON RECOVERED CLOCK OF THE CDR WITH PROPOSED VCO

Parameters	with Noisy Power Supply		
Noise amplitude (mV) at 10MHz	50	100	200
Jitter, ps (%UI) on Recovered clock	23, (2)	34, (3)	57, (5)

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