Ultra-Low-Voltage Dual-Rail NAND/NOR for High Speed Processing

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***Abstract*—This paper expands Ultra-Low-Voltage Dual-Rail (ULVDR) technology to 2-input logic gates. While previous research has been focused on inverters, it is important to investigate and demonstrate the function and speed of ULVDR in bigger, more complex circuits. ULVDR offers a significant speed increase over the more traditional Cascode Voltage Switch Logic (CVSL). Using the industry standard 90 nm CMOS process and a supply voltage of 300 mV, ULVDR NAND gates are more than 50 times faster than CVSL, when comparing chain evaluation delay.**

Keywords–Ultra-Low-Voltage; high-speed; ULVDR; NAND; CVSL.

I. INTRODUCTION

Over the past 30 years, electronics have become faster, cheaper and much more prevalent. This has pushed the industry towards smaller devices with lower supply voltage, as well as power consumption. As feature sizes approach a few atoms in length, further miniaturization becomes impossible.

Wearables, as well as smaller smart / Internet of Things (IoT) devices, are becoming much more common. All these devices can be powered by batteries and/or various means of energy harvesting. Either way the circuits need to be energy efficient and possibly operate at lower supply voltages. Within energy harvesting the supply voltage domain ranges from $175\,\mathrm{mV}$ to $350\,\mathrm{mV}$, which is often referred to as Ultra low Voltage. Exploring alternate circuit topologies is the most accessible way to reduce supply voltage and power consumption while maintaining speed. New circuit topologies can be manufactured using existing factories and technology are favorable. Completely new ways to build computers inspired by biology or quantum physics are still far away from competing with the silicon electronics industry.

A prominent new logic style which builds on CMOS [1], CVSL [2] and domino logic [3], namely the ULVDR inverter, is stated to be 25 times faster than traditional dual rail clocked CVSL [4]. Our work in this paper contributes to the field of Ultra Low Voltage ($300\,\mathrm{mV}$) and is based on the design logic presented in [4]. In this paper, we present a ULVDR NAND/NOR gate.

The content of this paper is as follows: In Section II, we introduce the ultra low voltage dual rail CVSL logic style. The ULVDR NAND/NOR gates with transistor details are discussed in Section III with the simulation verifying the logic is presented in Section IV. In Section IV-D, we compare our design to a CVSL gate with the simulation environment of a chain. Finally, a conclusion is included in Section V.

II. ULTRA LOW VOLTAGE DUAL RAIL LOGIC

A ULVDR precharge to 1 (**0P1**) inverter is shown in Figure 1. (A **0P1** gate has low voltage on inputs and high voltage on outputs, during precharge). At $300\,\mathrm{mV}$, the delay of a ULVDR inverter has been demonstrated to be 7% of the CVSL inverter delay [4].

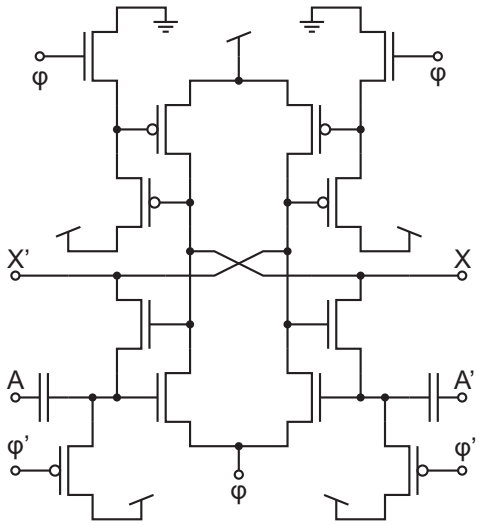

Figure 1. ULVDR 0P1 Inverter

During precharge:

When φ is high, the inverter is in precharge and not evaluation. Recharge transistors set all floating gates to their active state, such that both precharge (P) and evaluation (E) transistors are conducting. The output is brought to the precharge voltage, $300\,\mathrm{mV}$ for 0P1 and $0\,\mathrm{mV}$ for 1P0. Keeper(K) transistors do not play a significant role during precharge.

During evaluation:

When φ is low, the inverter is in evaluation. Recharge transistors are turned off, allowing the gate nodes of precharge (P) and evaluation (E) transistors to float. This is called a floating gate. When the input rising edge arrives, capacitive coupling causes the evaluation transistors floating gate to be supercharged, achieving voltages outside $0 \leq V_{GS} \leq 300\,\mathrm{mV}$.

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The output switches quickly, and the keeper (K) transistors discharge the floating gate, turning the evaluation and precharge transistors which should not be conducting completely off.

For example, on a precharge to 1 inverter, a gate voltage, $V_{GS} \approx 550\,\mathrm{mV}$ allows the output to quickly transition to 0. Digital circuits limited to gate voltages within $0 \leq V_{GS} \leq 300\,\mathrm{mV}$, like CVSL and CMOS, are much slower as the transistors are only weakly conducting in this sub-threshold state. At $300\,\mathrm{mV}$, the delay of a ULVDR inverter has been demonstrated to be 7% of the CVSL inverter delay [4].

III. NAND GATES

A. CVSL NAND gate

CVSL technology is used for comparison. Figure 2 shows a static CVSL NAND. At $300\,\mathrm{mV}$, the CVSL has similar speed to a static CMOS.

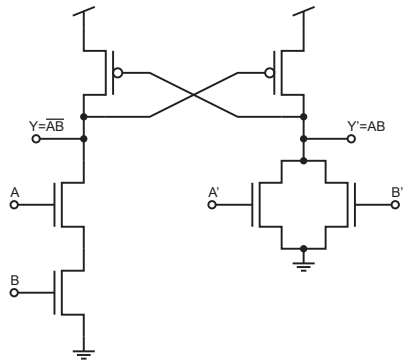

Figure 2. Static CVSL NAND used for comparison

In CVSL, when the input(s) arrive, one pull-down nMOS network is active. This pulls the output down to low, which in turn activates the pull-up pMOS transistor of the other output. As the other output goes high, the pMOS transistor of the first output is turned off, eliminating static power consumption. After some amount of time, an evaluation delay, one pull-down nMOS network is active, and the other pull-up pMOS transistor is active.

Sizes used for CVSL NAND gates are shown in Table I. Transistors are sized using $W/L = 120\,\mathrm{nm}/240\,\mathrm{nm}$, finger count, $N = 1$ with exceptions listed in Table I. n and p are used to specify nMOS and pMOS transistors. $\|$ and s are used for sizes applying to parallel and series transistors, respectively. This circuit was simulated for all possible input combinations, and average delays were computed. $t_{df\mu}$ and $t_{dr\mu}$ are the average delays (falling and rising edge on output). Note that the rising edge is much slower than the falling edge, due to the relatively weak pull-up pMOS.

B. ULVDR NAND

A ULVDR NAND gate was created based on the CVSL NAND (Figure 2) and ULVDR Inverter (Figure 1). The evaluation transistors were substituted by parallell($\|$) and series(s) evaluation resistors. The precharge circuitry was duplicated to accomodate for the two floating gate inputs. Figure 3 shows both versions of the ULVDR NAND/NOR gate.

TABLE I. CVSL NAND DIMENSIONS

Variable:	Value:
W	120 nm
L	240 nm
$N_{n\|}$	2
N_{ns}	4
t_{ie}	1 ps
$t_{df\mu}$	0.826 ns
$t_{dr\mu}$	6.80 ns

When designing ULVDR gates and setting transistor dimensions it is important to consider the state of the circuit once evaluation starts. Before the inputs arrive, all precharge and evaluation transistors are active, with gate to source voltages, $|V_{GS}| \approx 300\,\mathrm{mV}$. Thus, the output will be pulled by the evaluation networks away from the precharge value. It is important to dimension precharge and evaluation transistors to be at equilibrium around 90% of the precharge value. This was done by Mirmotahari, Dadashi, Azadmehr, *et al.* in [4] and those sizes are used as a starting point. As the ULVDR inverter has symmetric rails (sides) it is enough to do one such matching per circuit.

TABLE II. ULVDR NAND DIMENSIONS

0P1	
Symbol:	Value:
C	7 fF
W	120 nm
L	100 nm
L_{pP}	240 nm
W_{nE}	240 nm
$N_{nE\|}$	1
N_{nES}	2
$N_{pP\|}$	8
N_{pPS}	4

1P0	
Symbol:	Value:
C	11 fF
W	120 nm
L	100 nm
L_{nP}	240 nm
$N_{nP\|}$	2
N_{nPS}	1
$N_{pE\|}$	1
N_{pES}	2

For the ULVDR NAND/NOR gate, each rail is different and requires separate matching. Series evaluation transistors are doubled in size (finger count, N) to account for increased series resistance. Precharge transistors connected to parallel evaluation transistors are also doubled, to account for the increased parallel conductance. New transistor dimensions can be found in Table II. Recharge and keeper transistors are minimum sizes, but can be scaled according to timing requirements.

IV. SIMULATION

A. Logic verification

Figure 4 shows the NAND gate response to a binary counting sequence. Stimuli sequence 00, 01, 10, 11 produces the familiar NAND response; 1, 1, 1, 0. A1, B1 and X1 are the noninverted signals, A2, B2 and X2 are their respective compliments.

The transient in Figure 5 shows the evaluation transistor floating gate voltage, FGA1, quickly jump when the input arrives. It peaks at $565.44\,\mathrm{mV}$ allowing the nMOS transistors to rapidly pull the output down to 0.

B. Parasitic delay

Using identical inputs, and ideal clock and voltage sources, parasitic delays were simulated. Delay was measured from input switches to output switches (50% to 50%). Another gate

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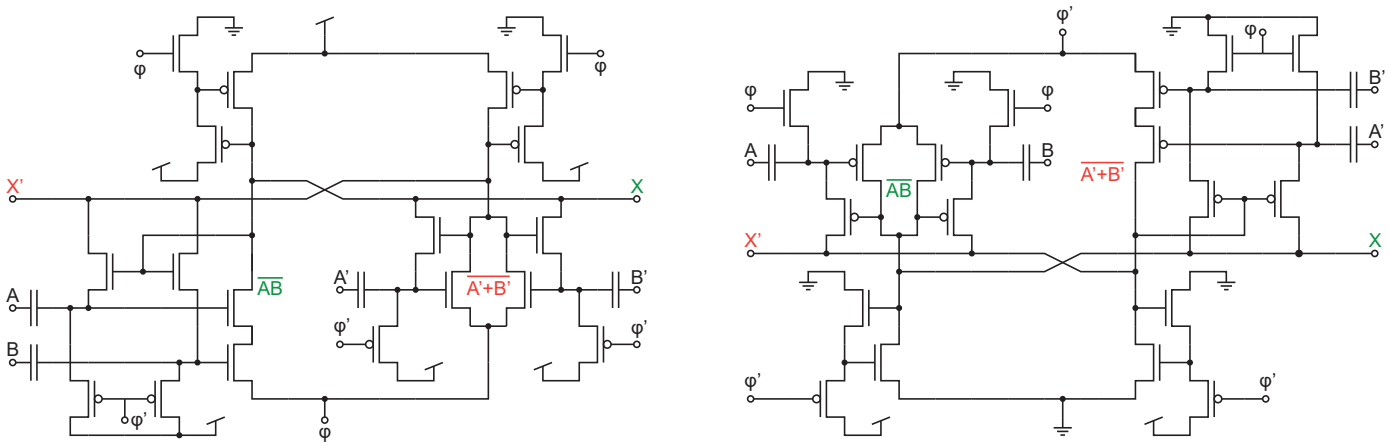

Figure 3. ULVDR NAND; 0P1(left), 1P0(right)

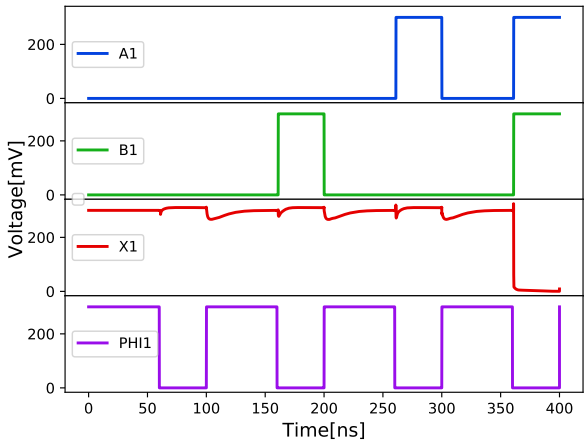

Figure 4. ULVDR NAND 0P1 response to 4 different inputs

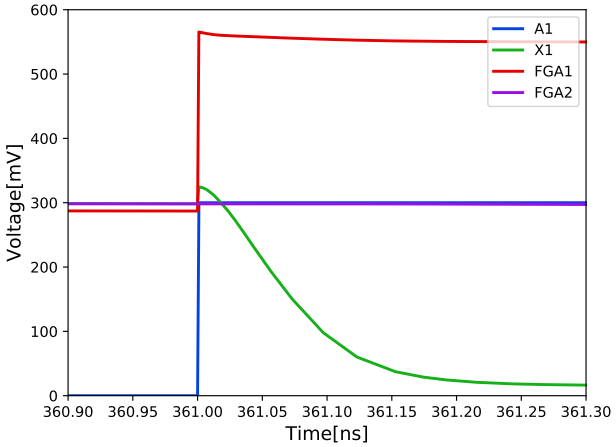

Figure 5. Floating gate voltage when ULVDR NAND is switching

was connected to the output as a semi-realistic load (opposite polarity for ULVDR). Table III shows the results for both CVSL and ULVDR gates.

TABLE III. PARASITIC DELAYS (WORST CASE AND AVERAGE)

	CVSL NAND:	ULVDR NAND:
t_e	1 ps	1 ps
t_{dw}	9.032 ns	0.178 ns
$t_{d\mu}$	6.796 ns	0.103 ns

When using ideal inputs and supply (300 mV) the ULVDR gates have parasitic delays ranging from 32.1 ps to 178.0 ps. The average parasitic delay for ULVDR NAND gates is approximately two orders of magnitude smaller than for CVSL. These ideal characteristics are useful for comparison, but not realistic - Section IV-D shows a better delay estimate, using chain delay.

C. Monte Carlo simulation

A 200 sample Monte Carlo Sweep was run to show the effects of mismatch and process parameters (variance). The results for both CVSL and ULVDR NAND gates are shown in Figure 6. Both plots are on the same time scale.

D. Chain delay

In Section IV-B, parasitic delay was estimated. An ideal input signal gives lower parasitic delay than what you can expect in a real circuit. A more realistic delay can be estimated using a chain of NAND gates. In this configuration the NAND gates act as inverters. There are 2 logic states, either the input (and ouptut) is low, or high. As there are 2 versions of the ULVDR gate the delays for these states differ.

Figures 7 and 8 show transients from the chain delay simulations. Two cases were simulated, $00 \rightarrow 11$ and $11 \rightarrow 00$.

V. CONCLUSION

The CVSL NAND gates achieve an average (per gate) delay of 9.658 ns and 9.738 ns. (For the two simulation cases mentioned in Section IV-D.) The ULVDR NAND chain has a

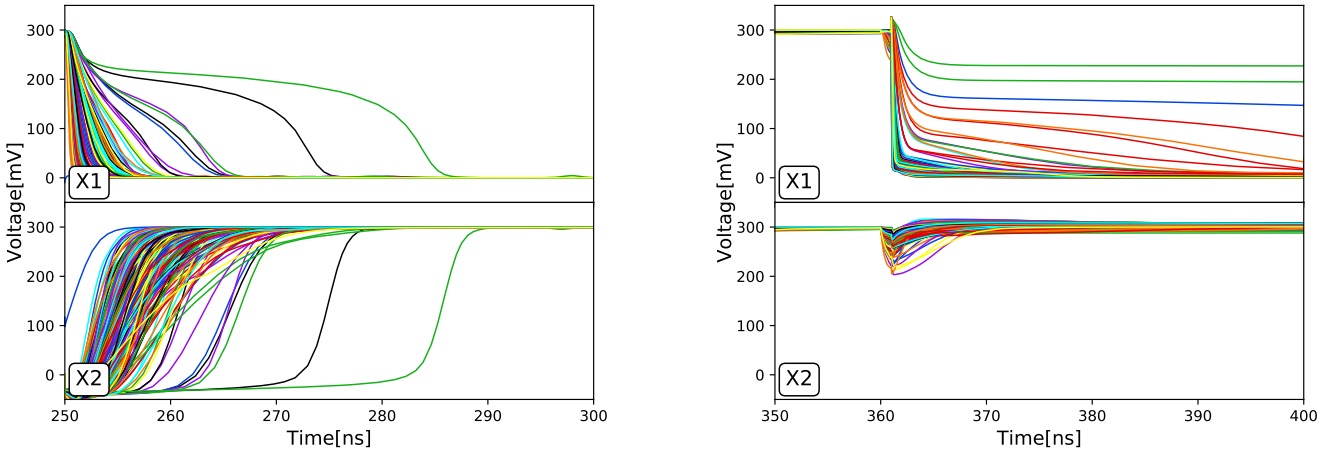

Figure 6. Monte Carlo simulation; CVSL NAND (Left), ULVDR NAND (Right)

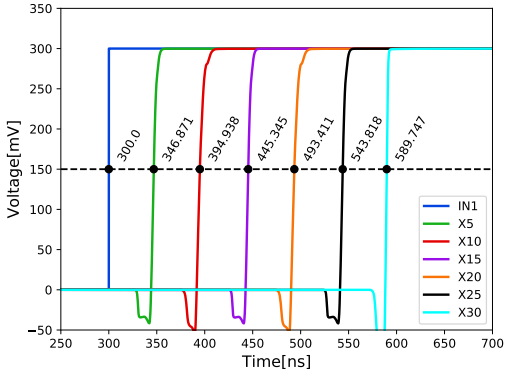

Figure 7. Output delay for chain of 30 CVSL NAND gates

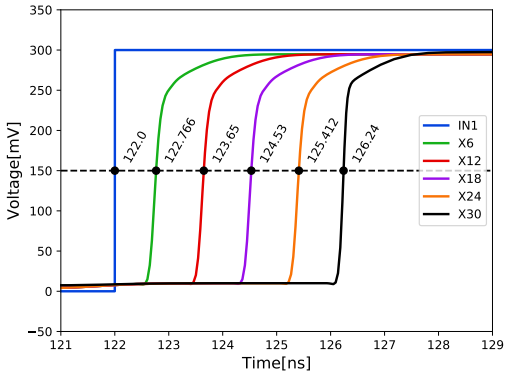

Figure 8. Output delay for chain of 30 ULVDR NAND gates

per gate average delay of 169.705 ps and 141.33 ps. A speedup factor, s, can be calculated (worst case delays used):

$$s = \frac{t_{\text{CVSL}}}{t_{\text{ULVDR}}} = \frac{9.738\,\text{ns}}{0.169\,705\,\text{ns}} \approx 57$$

The chain test in Section IV indicates that ULVDR NAND gates can be more than 50 times faster than static CVSL NAND gates. The tradeoff is the complexity and size in silicon, especially when considering necessary clock and precharge circuits. This paper does not consider power usage, layout, clock drivers, etc. Further research is needed to completely characterize the ULVDR NAND gate and the differences between ULVDR and CVSL in terms of power, speed, robustness, area, etc.

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