Design of QCA Full Adder for Multiplier Circuit

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***Abstract*—A quantum-dot cellular automata (QCA) is one of the circuit design technology in next generation. It has advantages of nano-sized devices and low power consumption. A multiplier is used in various fields and one of the most important circuits in processor. Multiplier is consisted of AND gates and full adders. In this paper, we design a small-sized 1-bit full adder for an efficient QCA multiplier. The proposed circuit is simulated using QCADesigner tool.**

Keywords-nanotechnology; quantum-dot cellular automata; multiplier; full adder

I. INTRODUCTION

Quantum-dot cellular automata (QCA) refers to quantum computational models that have been devised in the same way as existing models of cellular automata introduced by Von Neumann. QCA is as a candidate to replace complementary metal-oxide-semiconductor (CMOS) technology and it attracts much attention with very small even number molecules or atomic scale and low power consumption [1].

Many circuits have been proposed and simulated [2-5]. One of these circuits, the multiplier receives binary data as input and outputs it. A multiplier is necessary for most processors, and since the circuit configuration is more complex than other operations in the processor, depending on the performance of multiplier circuit, the speed of the system can be affected. A multiplier consists of AND gates and full adders. In QCA, an AND gate can be designed by using a majority gate, but full adders have various circuit design methods. Since the design of an efficient full adder can improve the performance of the multiplier, many full adders have been proposed in the QCA. In this paper, we propose an efficient 1-bit full adder by using a majority gate and a 3-input exclusive-OR (XOR) gate.

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II. RELATED WORK

Fig. 1 shows a QCA cell and wire. A QCA circuit consists of quantum cells with four quantum dots. The quantum cell of Fig. 1 (a) has two electrons that can tunnel between the quantum dots, and the electrons are located diagonally from each other by the Coulomb repulsion. The quantum cell has a value of 1 (1) or -1 (0) depending on the position of the electrons. A quantum cell affects adjacent cells by coulomb repulsion. Therefore, the same value propagates along the straight line as shown in Fig. 1 (b). A QCA wire and a majority gate can be designed using the coulomb repulsion between the cells [6]. The majority gate in Fig. 2 is a circuit that determines the output value by majority vote from three inputs. By using this circuit, it is possible to design an AND gate and an OR gate which are the basis of the logic circuit. If one input value is fixed to 1, then the majority gate performs as an OR gate, and if one input value is fixed to 0, then it performs as an AND gate [7]. An AND gate is needed to compose a full adder, and the AND gate computes and outputs with fixed value of 0 and two inputs.

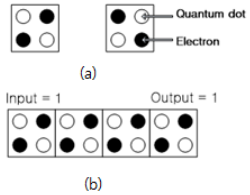

Figure 1. QCA basic concept: (a) QCA cell and (b) QCA wire based cells

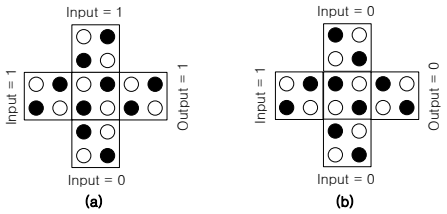

Figure 2. Two types of majority gates: (a) majority gate (output is 1) and (b) majority gate (output is 0)

III. PROPOSED QCA FULL ADDER

In this section, we describe a proposed 1-bit full adder. The proposed circuit is 1-bit full adder and is designed using a majority gate and 3-input XOR gate. The majority gate is used as an AND gate and outputs Carry among the outputs of full adders. The 3-input XOR gate is a modified form of the previous 5-input majority gate [8] and outputs Sum.

Figure 3 shows a 1-bit full adder block diagram. Inputs A, B, and C output Carry through the majority gate and Sum through the 3-input XOR gate. Fig. 3 shows a 1-bit full adder

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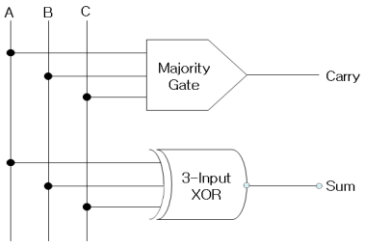

Figure 3. A block diagram of 1-bit full adder

TABLE 1. TRUTH TABLE OF 1-BIT FULL ADDER

Input			Output	
A	**B**	**C**	**Carry**	**Sum**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

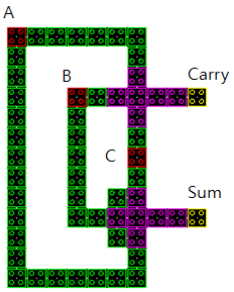

Figure 4. QCA layout of the proposed 1-bit full adder

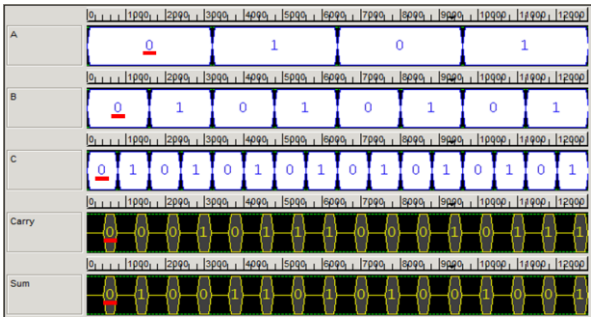

Figure 5. Simulation result of proposed circuit

block diagram. Inputs A, B, and C output Carry through the majority gate and Sum through the 3-input XOR gate. Table 1 is a truth table of 1-bit full adder. The input values are binary bits 000 to 111 and are the same as the simulation result of the proposed QCA full adder.

Fig. 4 shows the circuit layout of the proposed QCA 1-bit full adder. In order to efficiently connect the wiring of the input values on the QCA, the wiring is designed so that one input propagates the signal in both directions respectively. The 3-input XOR gate connected to the output Carry and the 3-input XOR gate connected to Sum are similar in shape, but are modified with the existing 5-input majority gate by adding two cells to the intersection cell diagonal [8]. Fig. 5 shows simulation result of our proposed full adder circuit using QCADesigner tool version 2.0.3. It shows a clear strong signal and the result is consistent with the truth table in Table 1. Three inputs are shown as a blue line on white background and two outputs are as a yellow line on black background in Fig. 5.

IV. CONCLUSIONS

In this paper, we design a new 1-bit full adder with majority gate and 3-input XOR gate in QCA. In the proposed circuit, the wires connected to the input value are designed to propagate in both directions. The proposed circuit is a planar circuit and proposed for the purpose of designing a planar multiplier.

ACKNOWLEDGMENT

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