Novel High Speed and Robust Ultra Low Voltage CMOS NP Domino NOR Logic and its Utilization in Carry Gate Application

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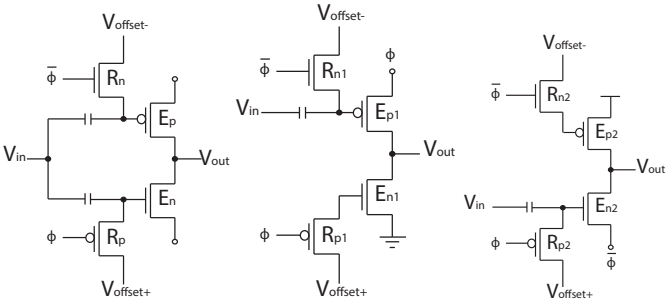
***Abstract*—This paper is based on two parts. In Part 1, we shall present a new Ultra Low Voltage Static differential NOR topology. This will show how Ultra Low Voltage circuits are designed and what are the pros and cons of these circuits. In Part 2, utilizing the design presented in Part 1, we shall present a novel design of an Ultra Low voltage Carry Gate. This shall emphasize the use of such design in an application such as carry gate. The Ultra Low Voltage topologies presented in Part 1 are well known for their high speed relative to conventional CMOS topologies regarding subthreshold operation. The main objective is to target the robustness of the presented ciruits. We shall also imply as to what extent these circuits can be improved and what their benefits, compared to conventional topologies, are. The design presented in Part 2, compared to a conventional CMOS carry gate, is area efficient and high speed. The relative delay of a Ultra Low Voltage carry gate lies at less than 3% compared to conventional CMOS carry gate. The circuits are simulated using the TSMC 90nm process technology and all transistors are of the Low Threshold Voltage type.**

***Index Terms*—ULV; Carry Gate; NP domino.**

I. Introduction Part 1

Technology, being an important factor of the modern civilization, has been facing challenges enormously in every aspect. Demand for low power and faster logic pursue an overwhelming position in modern electronic industry. As the industrial demand grows for the CMOS transistor, from time to time it needs to go through rehabilitation process accordingly. However, as the Moores law suggests, advancement in CMOS technology, in the means of dimension scaling has almost hit a barrier for a number of reasons. The most important one is power dissipation at the smaller dimensions of the transistor. To overcome this problem, a number of approaches have been proposed [1][2]. Scaling supply voltage (V_{DD}), being prominently the most effective, has been proposed and adopted by many [3][4][5]. However, scaling supply voltage has an adverse affect on the performance of the CMOS circuits as it decreases the ON current I_{ON} and hence the speed.[6] presents a solution to this problem by employing floating gate Ultra Low Voltage (ULV) design, which raises the DC level of the input floating node even more than the supply voltage itself and thereby increasing the I_{ON}.

Floating-gate is achieved by connecting a capacitor at the input of the transistor gate. This isolates the gate terminal electrically, i.e., no DC path to a fixed potential. Such a gate is called non-Volatile Floating-gate. Given that the transistor dimensions are smaller than 0.13 μm and gate oxide is less than $70AA\frac{1}{2}$, there shall be a significant gate leakage current. To avoid this leakage, frequent initialization of the gate is required. This can be achieved by connecting floating gates of the NMOS input transistor and PMOS input transistor to, a fixed potential, i.e. through a PMOS to the Voffset+ and through NMOS to the Voffset- respectively. This approach, first presented in [4], is called semi-floating gate (SFG) and has been used in this paper. In Section I-A, a brief introduction to ULV design is presented. Section II, presents, first, a Non-differential circuit proposed in [7] and thereby presents a new solution to the problem encountered in non-differential ULV circuit by designing a new NP domino static differential ULV NOR. In Section III, we shall present the simulation results of all the ULV circuits and Dual Rail domino NOR relative to conventional NOR.

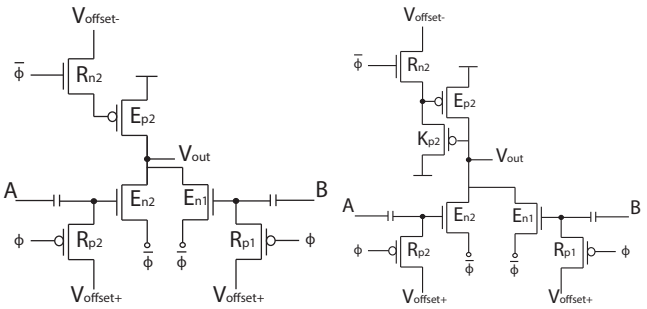


(a) A simple SFG-ULV inverter (b) P-type inverter (c) N-type inverter

Fig. 1. SFG NP ULV domino inverter.

A. ULV Inverter

1) Evaluation and Precharge Phase: A simple ULV inverter model is presented in the Figure 1a. A ULV SFG circuit design consists of two phases. An evaluation phase, determined by the evaluation transistors E_n and E_p, and a precharge phase determined by the precharge transistors R_n and R_p. As seen in the Figure 1a inverted clock ($\overline{\phi}$) is applied to R_n and clock (ϕ) is applied to R_p. In such a circuit, the precharge phase occurs when ϕ=0 and the circuit enters evaluation phase when ϕ=1. During the precharge phase, the input floating nodes are charged to a desired level, i.e, logical 1 or V_{DD} for the E_n floating gate and logical 0 or Ground



(a) N-type ULV Dynamic NOR (b) N-type ULV Static NOR

Fig. 2. NP domino dynamic and static ULV NOR gate.

(GND) for the E_p floating gate. No input transition occurs during the precharge phase. However, once the clock shifts from logical 0 to 1 and has reached a stable value of 1, an input transition may occur, which determines the logical state of the circuit's output. We can engage the circuit in an NP domino chain by connecting the source terminal of E_n to $\overline{\phi}$ (where $\overline{\phi}$=1 during the precharge phase) and the source terminal of the E_p to V_{DD}. Such a configuration gives us a precharge level of logical 1 and is called an N-type circuit. On the other hand, if we connect the source terminal of E_n to GND and the source terminal of the E_p to ϕ we can obtain a precharge level of 0. Such a configuration is called a P-type circuit.

Considering the example of N-type inverter, we know that the output of the N-type is precharged to 1. Once ϕ shifts from 0 to 1, circuit enters the evaluation phase. During the evaluation phase, there are two possible scenarios. If no input transition occurs, the output shall remain unchanged and hold its value to 1. Indicating that no work is to be done. However, if an input transition occurs and input is brought to 1 the E_{n2} shall be turned on and the output shall be brought to logical 0 or close to 0. This indicates that the only work to be done during the evaluation phase is to bring the output from 0 to 1 when an input transition occurs.

We have seen that the only work that is to be done, during the evaluation phase, is to bring the output to the logical 0 when an input transition occurs. This suggests that E_{p2} does not require an input transition at any stage. Therefore, we can remove the input capacitor of E_{p2}. Such a configuration can be called pseudo SFG ULV inverter and is shown in Figure 1c. An equivalent P-type Pseudo SFG ULV inverter is shown in Figure 1b. This will lead to load reduction and hence higher speed. However, we may encounter some robustness issues with respect to noise margin due to leakage current.

II. Methods

A. Non-differential ULV NOR circuit

A Non-differential Dynamic ULV NOR (DULVN) and Static ULV NOR (SULVN) gate is shown in Figure 2. Recall configuration of ULV inverter. The only difference in configuration of ULV NOR circuit is that, in order to obtain a P-type DULVN, we have to apply an extra input at the evaluation transistor E_{p1} in a P-type inverter. In order to obtain N-type DULVN employ an extra evaluation transistor E_{n1} in parallell with E_{n2}.

The SULVN is configured in the same manner as the DULVN. However, we add keeper transistor in the described configuration. An NMOS keeper is connected to the floating gate of E_{n1} and a PMOS keeper is connected to the floating gate of the E_{p2} in P-type and N-type SULVN, respectively. However, these circuits are prone to some noise margin (NM) issues due to precharged input floating nodes that holds it's value under evaluation phase. Thereby resulting in short circuit leakage current. In order to solve this problem, let us consider an example of N-type DULVN. Discharging of the floating gate of the $E_{n1/n2}$, when no input transition occurs, and charging of the floating gate of the E_{p2} with V_{DD}, when an input transition occur, will ensure a better noise margin. This can be achieved by engaging keeper transistors at these nodes and connecting the source and drain terminal of the keeper transistors K_p and K_n, respectively, which may not interupt in precharging of the floating gate and and still manages to discharge these nodes under evaluation phase when required. A problem with such a circuit is the potential false output transient if the input transient is significantly delayed compared to the clock edge [7]. Synchronization of the signals employed through the keeper transistors with the input may solve the problem.

B. Static differential ULV NOR

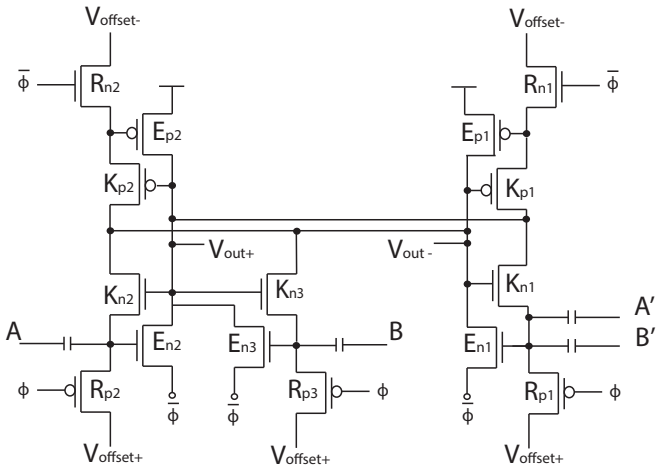
A static differential ULV NOR (SDULVN) gate will always have the same precharge level at the both outputs in the preacharging phase and differential outputs in the evaluation phase. A SDULVN gate is shown in Figure 3. We have connected outputs of the opposite ends, V_{out+} and V_{out-}, at the drain terminals of the both keeper transistors. In order to achieve maximum robustness, MTCMOS method is used, i.e, transistors in the path with critical timing has lower threshold voltage, to achieve the maximum speed, and transistor in the path with critical leakage issues has higher threshold voltage, to achieve the minimum leakage.

III. Simulation Result

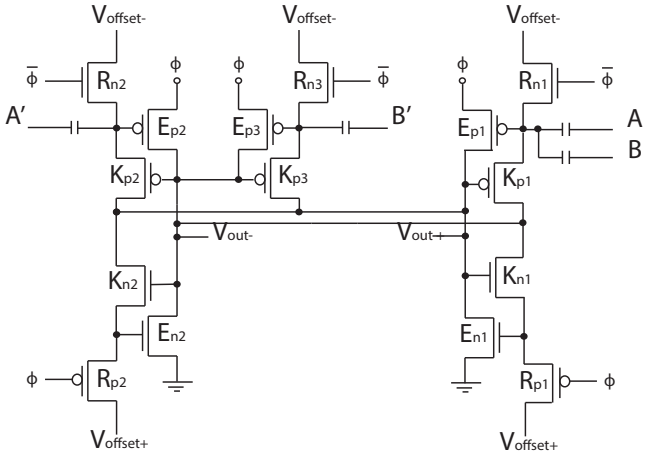
We have simulated four different topologies, conventional Dual Rail domino NOR, DULVN, SULVN and SDULVN each with a load of FO1. Worst case scenario for three ULV topologies, considering delay, is when both inputs has opposite logical values and considering power and NM is when the output holds the precharged value under evaluation phase.

A. EDP and PDP of Dynamic, Static, Differential ULV topology and dual rail domino NOR

It is suggested in [3] that in subthreshold regime the transistor may operate as a current source, hence switching the output. Author suggests that the transistor may work as a current source for as little as 100 mV at room temprature.



(a) Static differential N-type ULV NOR^2/NAND^2.



(b) Static differential P-type ULV NOR^2/NAND^2.

Fig. 3. Static Differential NP ULV NOR.

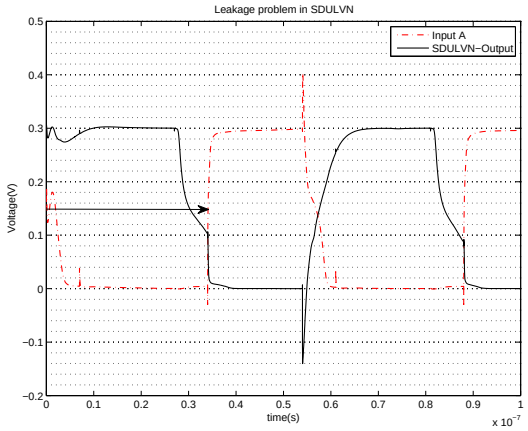


Fig. 4. Output of SDULVN where input is delayed and the output tends to shift before input due to leakage current. The graph is taken from Monte Carlo simulation in order to show why the limits for functional circuits are set as they have been discussed. Supply voltage at 300 mV.

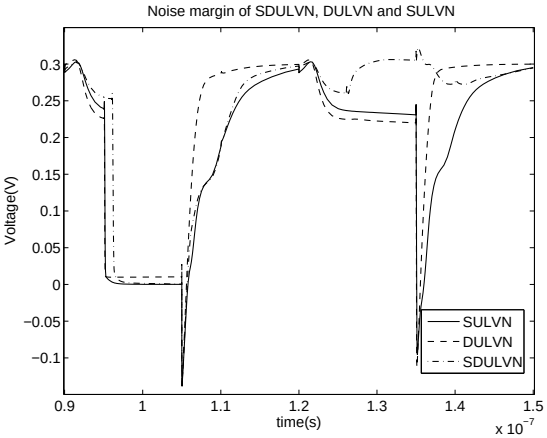


Fig. 5. Noise margin of SDULVN compared to DULVN and SULVN. Supply voltage of 300 mV.

So, before we start analyzing EDP and PDP for varied supply voltages, we have to set some limits that constitutes a functional circuit. Mentioned earlier, dynamic and static topologies suffers from current leakage problem. So as we increase the V_{DD} current leakage increase resulting in a non-functional circuit. However, this can be overcommed by strengthening down the transistor. SDULVN manages to integrate itself according to the input provided. So, even if the output is delayed and a leakage occur, at the arrival of input it will manage to change the output accordingly. However, if the leakage in device is greater than $V_{DD}/2$, we may not be able to measure a propagation delay. Figure 4 highlights the leakage problem, where a measurement of propagation delay is avoided due to early switching of the output. Thus, in order to achieve maximum robustness, we shall consider a circuit non-functional if the output of the circuit exceeds $V_{DD}/2$.

Figure 5 shows improved noise margin of differential topology with respect to dynamic and static topology at supply voltage of 300 mV. Keeper transistors manages to turn off the evaluation transistors when required. Consequently, SDULVN has 30% and 36% better noise margin in worst case scenario compared to SULVN and DULVN, respectively. Delay of ULV NOR topologies relative to conventional NOR can be seen in Figure 6. Average relative delay of SDULVN lies at 6%, i.e, to switch an output SDULVN consumes 6% of time consumed by a conventional NOR to switch an output. Figure 7 shows the PDP of three ULV topologies. It shows that ratio between the relative delay and relative power normalizes itself to unity at some supply voltages yet SDULV wins at most of them. EDP graph shown in Figure 8 again displays enhanced speed of the ULV topologies overcomes exaggerated power dissipation.

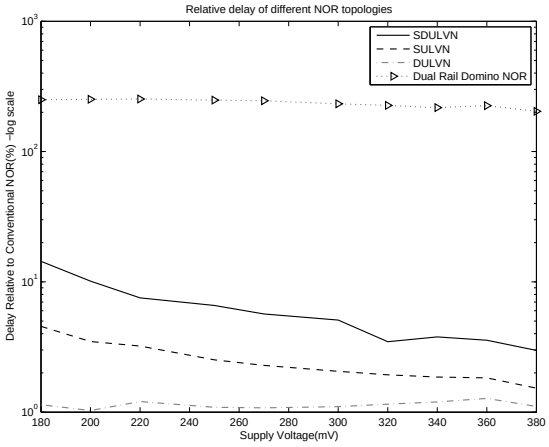


Fig. 6. Relative delay of three ULV topologies Dual Rail domino NOR to conventional NOR.

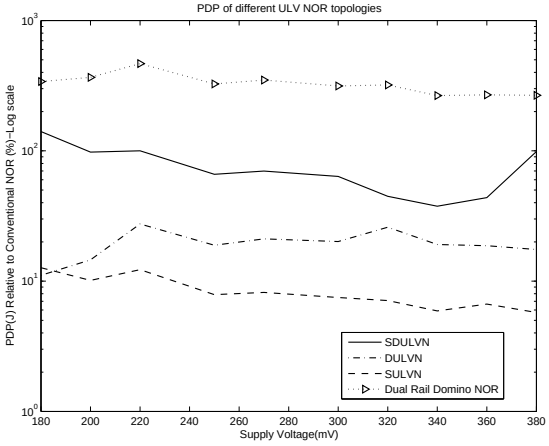


Fig. 7. Relative PDP of three ULV topologies Dual Rail domino NOR to conventional NOR.

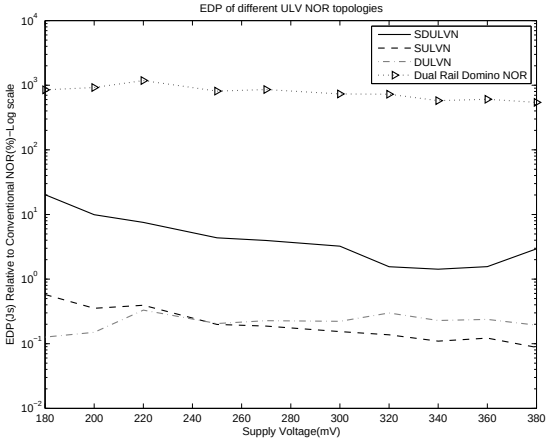


Fig. 8. Relative EDP of three ULV topologies and Dual Rail domino NOR to conventional NOR.

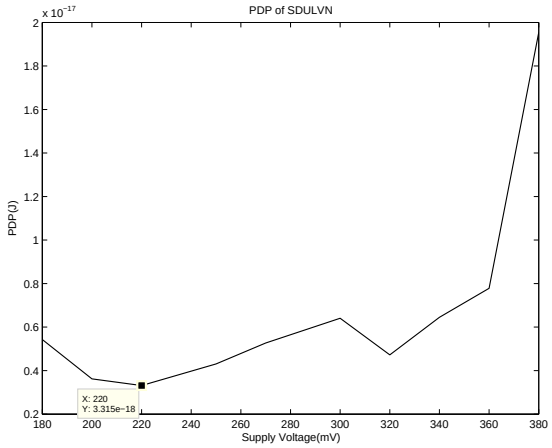


Fig. 9. PDP of SDULVN. Graph shows the Mimimum Energy Point

B. Maximum and minimum Supply voltage and Minimum energy point

Threshold voltage for these low voltage transistor lies around 260 mV with normal strength. As we have strengthen up the evaluation transistor, threshold point decreases. So, we can see from Figure 9 that minimum energy point of differential topolgy lies around 220 mV. Taking into consideration our limits that constitutes a functional circuit we got minimum and maximum V_{DD} at 180mV and 380mV, respectively.

C. Process and mismatch variation

Attributes of a transistor at 90nm process suffers from variation under fabrication. Such variations can be of two types, inter-die, where all the transistors are printed on one die and may be shorter than normal because they were etched excessively, and intra-die, where number of dopant atoms implanted varies from neighboring transistor [8]. A change in behavior of the circuit can occur due to variation in V_t and channel length. Therefore, it is important to highlight this variation in any circuit. In order to obtain an idea of how robust a circuit tends to be toward process and mismatch variation, Monte Carlo simulation environment is the best solution to apply. A number of precautions can be taken to avoid further variation. Such as sizing up transistors, carefull layout design and so on. Law of Large number indicates that the larger the number of trials the closer it would be to expected value. Therefore, the number of simulations in Monte Carlo should be high as possible. We have used 100 simulations to mark the mean value.

D. PDP, EDP and minimum energy point results in Monte Carlo environment

Figure 10 shows that the minimum energy point shifts from 220 mV to 250 mV due to process and mismatch variation. As stated earlier V_t varies due to random number of dopant atom. This results in slight randomness in behavior of the

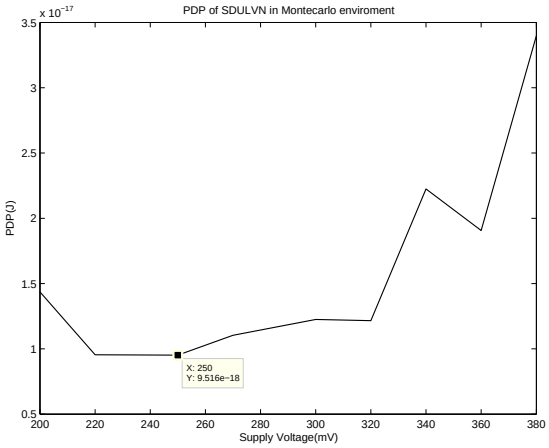


Fig. 10. PDP of SDULVN in Monte Carlo environment. Graph exhibits shift in Minimum Energy Point.

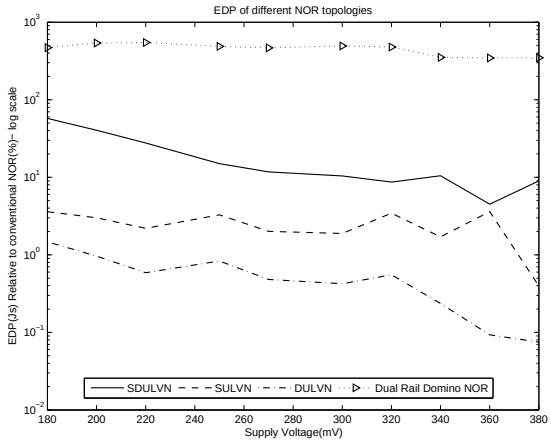


Fig. 12. Motecarlo simulation for EDP of three ULV topologies and Dual Rail domino NOR relative to conventional NOR.

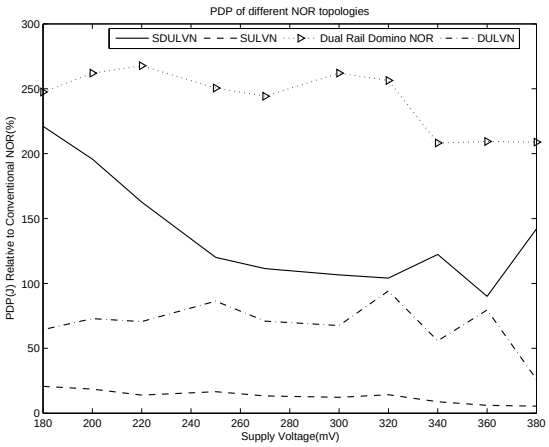


Fig. 11. Motecarlo simulation for PDP of three ULV topologies Dual Rail domino NOR relative to conventional NOR.

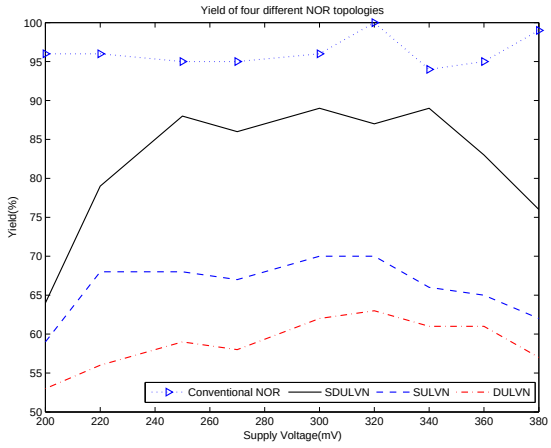


Fig. 13. Yield of SDULVN, DULVN, SULVN Dual Rail domino NOR and conventional NOR.

circuit and, therefore, results in shift in minimum energy point. Figure 11 shows PDP of three different ULV NOR topologies relative to conventional NOR and compared to Dual rail domino NOR. Figure 12 shows that EDP fluctuates from having relative mean value of 76% to 120% due to process variation.

E. Yield and 3σ EDP variation

As described earlier, we have to set a limit to differ between a functional and non-functional circuits. Considering those limits we have taken out graph for yield of all these circuits. Figure 13 shows that of ULV gates SDULVN has the best yield at an average of 82% yield compared to SULVN and DULVN, which have an average of 66% and 58% yield respectively.

$$PDP = V_{DD}^2 \cdot C \tag{1}$$

$$EDP = \frac{C^2 \cdot V_{DD}^3}{I} \tag{2}$$

As we know that objective of employing semi floating gate is to increase the current to increase the speed of the circuit. PDP is independent of current as shown in (1). Therefore, in order to obtain a variation that occurs due to higher current we have to focus on variation of EDP. Figure 13 shows 3σ variation of the EDP for four different NOR topologies. We can see that below minimum energy point of SDULVN the variation are alot higher than conventional topology. However, above this point, the EDP variation in SDULVN is better than Dual Rail domino NOR and almost at same level as in DULVN and conventional NOR.

IV. Conclusion Part 1

In Part 1 we have presented a new design for NP domino ULV NOR topology and demonstrated improvement in NM and yield. Although SDULVN topology has 2× the logic

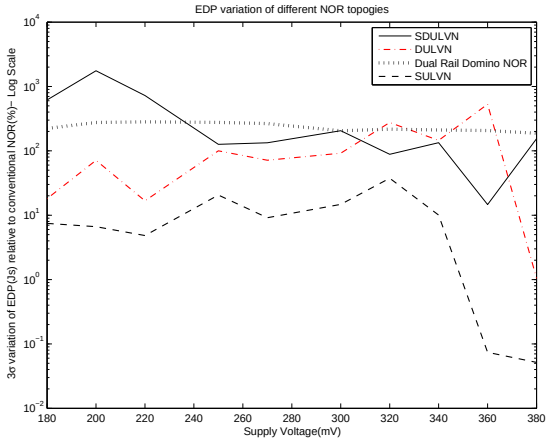


Fig. 14. 3σ variation of EDP for SDULVN, DULVN, SULVN relative to conventional NOR.

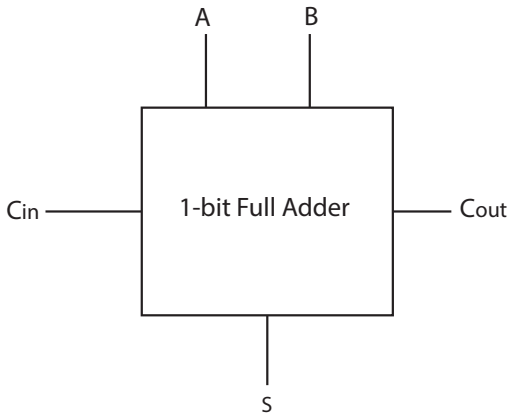


Fig. 15. 1 bit full adder

and almost $3\times$ complexity (number of transistor operate under evaluation phase) compared to conventional NOR, it is still $17\times$ faster. The output leakage problem encountered in SULVN and DULVN has been minimized by employing SDULVN design.

V. Introduction Part 2

As stated earlier, the demand for Ultra Low Voltage (ULV) circuits is increasing with the growth of the semiconductor industry. These circuits are being implemented in VLSI, where different kind of functions are combined on one chip. The Arithmetic Logic Units (ALU)s are one of the many circuits that are implemented in the VLSI chips. Since an adder is an important part of the ALU, the speed of the adder used, is important for the ALU's performance. The speed of the adder is determined by the propagation delay of the carry chain. Although high speed conventional carry circuits like Carry Look Ahead, Dual rail domino carry, CPL, etc., are well established design topologies, their performance suffers from degradation at ULV [9]. Several approaches are proposed for the improvement in performance [10][11] but the design presented in this paper is influenced by [12]. This paper shall present a new high speed NP domino ULV carry design. To highlight the improvement, the results shall be compared to conventional domino design such as Dual Rail Domino carry. In order to show as to what extent one is better than the other, regarding their speed and power, both the carry circuits are implemented in a 32-bit carry chain.

Section I-A presented a general introduction to the ULV circuits presented in [4]. Section VI presents different configurations of ULV carry designs and gives an explanation on how it works. Section VII presents the performance of the proposed ULV carry gate compared to the conventional carry gate.

VI. Methods

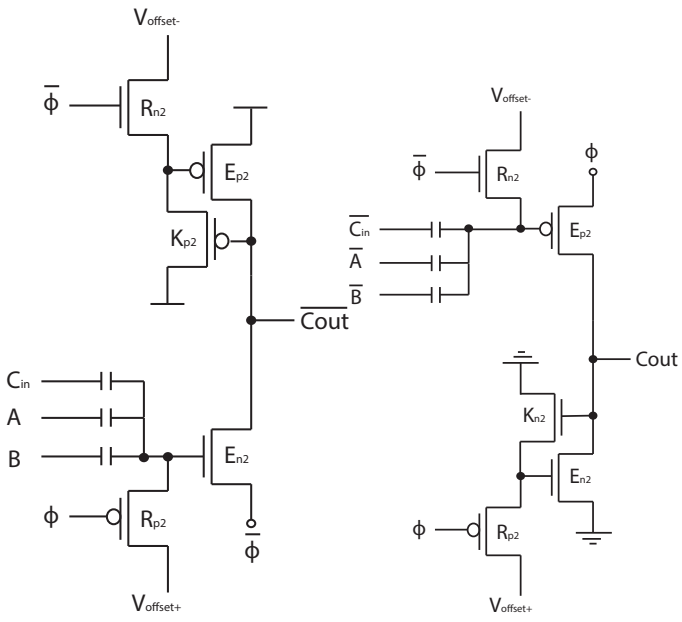
$$C_{out} = A \cdot B + (C_{in} \cdot (A \oplus B)) \quad (3)$$

The output of a carry circuit is generated using two inputs and a carry bit from the previous stage, if available (carry bit at the least signficant bit is always zero so it has no previous carry), as shown in Figure 15. Equation (3) shows an arithmetic approach to carry generation, where A and B is the input signal and C_{in} is the carry bit from the previous stage. There are two parts of this equation, one is generated internally, $A \cdot B$, and can be called carry generation (CG), the other one is dependent on the carry bit from the previous stage, $(C_{in} \cdot (A \oplus B))$, and is known as carry propagation (CP). The speed of any carry chain depends on the second part of this equation, because it has to wait for the carry bit from the previous stage to arrive. Inputs A and B both arives simultaneously at any stage of an N bit carry chain. Most conventional designs use two seperate parts for CG and CP but the design presented in this paper differs from the most designs as it is able to generate both CG and CP by applying all the inputs to a single transistor. This technique is called Multiple valued Logic (MVL), where classical truth value, logical 1 and 0, are replaced by finit or infinite logical values. It has a potential to decrease the chip area and total power dissipation [13].

A. Non-Differential Carry Gate

The Static Ultra Low Voltage Carry (SULVC) is a modified version of the ULV N-P domino inverter shown in Section I-A. The carry circuit uses a keeper, as proposed in [4], and 3 capacitors in parallel at the input gate providing the input logic for the circuit. The circuit is designed to make the input signals, A and B signal, cancel each other out when A and B have contrasting values to allow the carry input signal to determine the carry output in this case. Because of the cancellation requirement between the A and B signals they need to arrive as equally sized rising or falling transitions, this can be acheived by utilizing level-to-edge converters or a logic style with a VDD/2 precharge level.

If both A and B are rising, the floating node will rise causing a falling transition on the carry output of the N-



(a) N type SULVC. (b) P type SULVC.

Fig. 16. SULVC circuit.

TABLE I. TRUTH TABLE FOR A CARRY CIRCUIT

Inputs			Output
A	B	C_{in}	C_{out}
0	0	0	0
0	1	0	0
1	0	0	0
1	1	0	1
0	0	1	0
0	1	1	1
1	0	1	1
1	1	1	1

type circuit regardless of the carry input signal. If they are both falling, the carry input signal can not elevate the floating node voltage enough to cause a transition, leaving the carry output at precharge level. If A and B are not equal, their two transitions cancels each other out and the floating node remains at precharge level until a possible rising edge occurs on Cin. A P-type equivalent of the circuit is shown in Figure 16 (b), where all signals and logic are the inverse of those in the N-type circuit. For both circuits, a transition on the output indicates carry propagation and they can both be characterized as a carry generate circuit corresponding with the truth table shown in Table I, the transition logic for the N-type circuit can be seen in Table II.

During the precharge phase, the voltage level of the floating node is set to ground for the P-type circuit and V_{DD} for the N-type and can only be changed by the inputs through the capacitors in the evaluation phase. In these circuits, when used in CPAs (Carry Propagate Adder), C_{in} can arrive later than A and B when the carry bit has to propagate through the chain of carry circuits. This introduces the challenge of keeping the

TABLE II. TRANSITION TRUTH TABLE FOR N-TYPE SULVC

Inputs			Output
A	B	C_{in}	$\overline{C_{out}}$
↓	↓	0	1
↓	↑	0	1
↑	↓	0	1
↑	↑	0	↓
↓	↓	↑	1
↓	↑	↑	↓
↑	↓	↑	↓
↑	↑	↑	↓

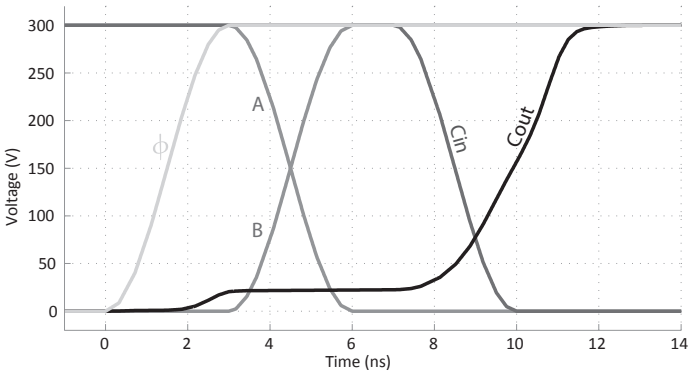


Fig. 17. Carry input and output for SULVC gate. Supply voltage at 300mV.

output precharge value during the evaluation phase in case no carry signal arrives. As Figure 17 shows, the floating node of the P-type circuit is precharged to 0V. This causes the transistor E_{p2} in Figure 17 (b) to conduct and the output will drift and may eventually cause an incorrect output value as shown in Figure 18 at 70ns. The drifting effect is countered with the K_{n2} and K_{p2} keeper transistors but the effect limits the length of the evaluation pase and therby the number of carry circuits that can be put in a chain and the maximum number of bits an adder based on the circuit can process in one clock cycle. The maximum achieved number of bits acheived varies with the supply voltage as shown in Figure 19 and at 300 mV a 32-bit carry chain can be implemented.

The transistor sizing is adjusted to accommodate the change

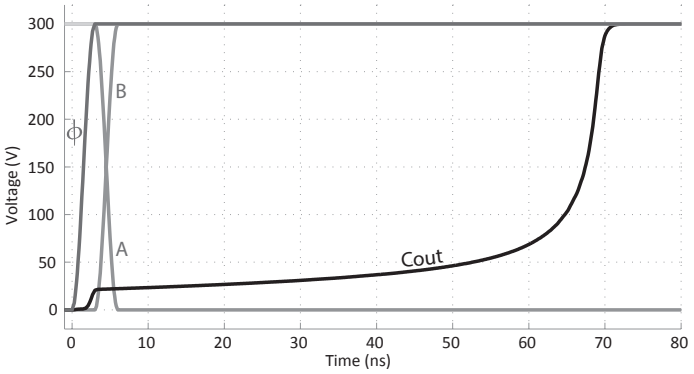


Fig. 18. Drifting problem of the SULVC output.

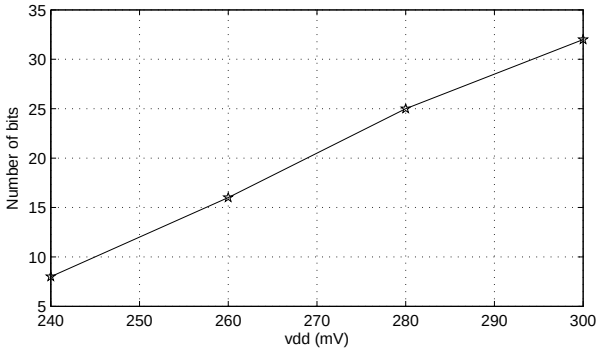


Fig. 19. Number of carry circuits or bit obtained from carry chain when supply voltage is varied.

in NMOS/PMOS mobility difference with changed supply voltage. In these simulations, the NMOS evaluation transistor size is kept minimum sized and the PMOS evaluation transistor length is changed to match the NMOS drive strength.

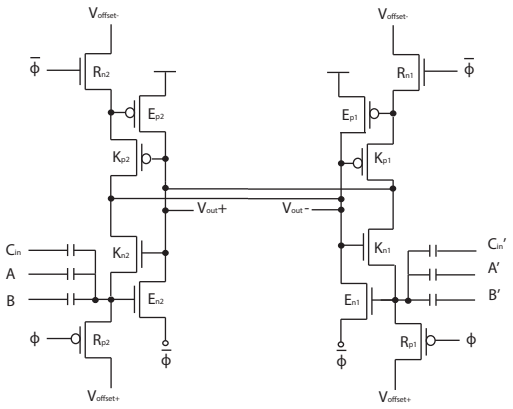
B. Differential Carry Gate

In order to overcome the challenges with robustness and drifting of the SULVC circuit, a differential approach is a possible solution. A Static Differential Ultra Low Voltage Carry (SDULVC) as shown in Figure 20 is designed in exactly the same manner as the SULVC, however, with differential inputs and outputs. The differential nature of the circuit makes it less prone to drifting and eliminates the need for level-to-edge converters it can be sized to allow a single edge without causing an output transition. The outputs of the proposed circuit are precharged to the same level during the precharge phase, however, it yields a differential output during the evaluation phase. So, instead of employing an inverter to obtain the carry bit we can read it from the opposite end of the circuit, i.e., in an N-type SDULVC if inputs A, B, and C are applied to E_{n2} output can be read from V_{out-}. Figure 20 demonstrates the design of an SDULVC circuit. The backgate of the keeper transistors of these circuits are connected to the floating gate to achieve maximum robustness.

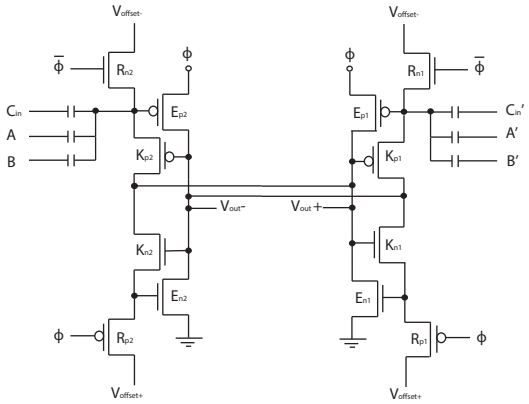
$$V_{fg} = V_{initial} + k_{in} \cdot V_{in} \text{where } k_{in} = \frac{\sum_{i=1}^{n} C_{innHigh_i}}{C_{total}} \quad (4)$$

The variable *'i'* in (4) denotes the index of the input and the *'n'* denotes fan-in. $V_{initial}$ is the precharge voltage level of the floating gate. C_{inHigh} is a combination of input capacitors with a high (rising) input.

Considering an example of an N-type SDULVNC, we can calculate the voltage level of the floating gate using (4). We assume that the diffusion capacitance is equal to the input capacitance and that the supply voltage is equal to the input voltage. The load capacitance introduced by the keeper's back-gate connection to the floating node should also be considered



(a) N type SDULVC.

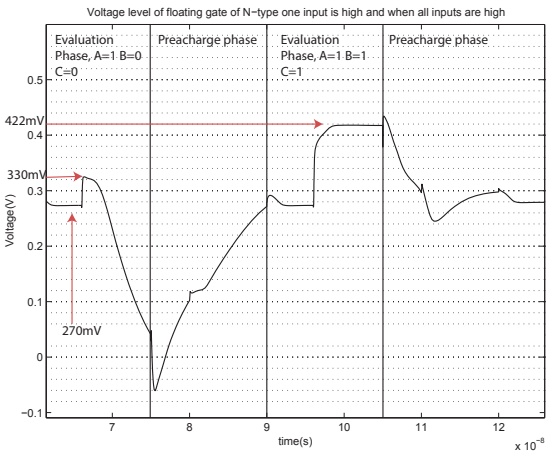


(b) P type SDULVC.

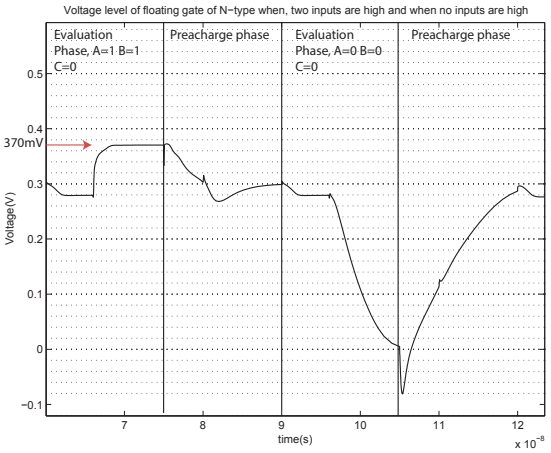
Fig. 20. SDULVC circuit.

and in this paper is assumed to be equal to the input capacitor as well.

Our calculation in (4) gives us a theoretical idea of the voltage level at V_{fg} (floating gate voltage). In the real world, the capacitance size might not be exactly the same as our assumption and depends on transistor size and many other factors like process variation and mismatch. The simulation results of the voltage levels for the floating gate in Figure 21 shows that the floating node is precharged to 270mV. Equation (4) yields an analytical result for the floating gate input of 330 mV, 390mV and 450 mV for one, two and three high inputs, respectivly. The simulation results in Figure 21a shows that the voltage level of the floating node gets to 330mV for a single rising input transition and to 420mV when all inputs are high. These results are marginally different from the calculated values. This is possibly due to the assumptions on capacitance sizes. Figure 21a shows that if only one input gets high, the keeper transistor turns on and discharges the floating node. The reason for this is that the transition at the input, i.e., 60mV, is not sufficient to produce enough current at the output. Figure 21b shows the results for two high inputs and all low inputs.



(a) Voltage level of input floating gate of an N-type SDULVC/SDULVC when A=1 B=0 and C=0, and when A=1 B=1 C=1.



(b) Voltage level of input floating gate of an N-type SDULVC/SDULVC when A=1 B=1 and C=0, and when A=0 B=0 C=0.

Fig. 21. Voltage level of floating gate of N-type at supply voltage of 300mV.

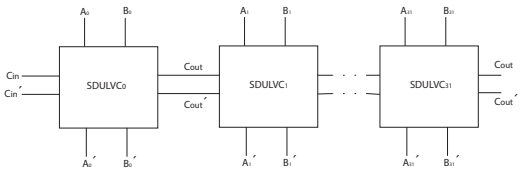


Fig. 22. 32 bit ULV carry chain.

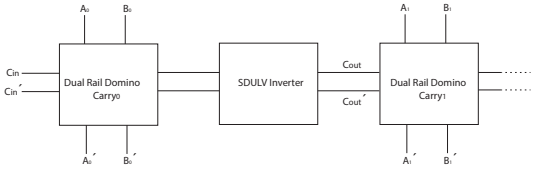
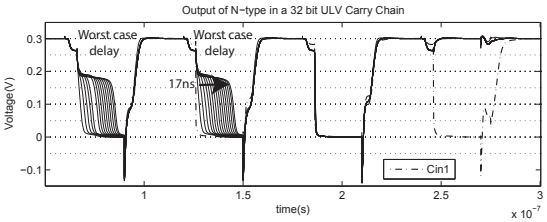
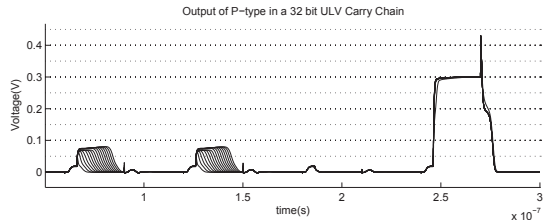


Fig. 23. Implementation of hybrid Dual rail domino carry.



(a) output ULV carry chain N-type.



(b) output ULV carry chain P-type.

Fig. 24. Simulation result of 32 bit ULV carry chain at a supply voltage of 300mV.

VII. Simulation

A. 32 bit SDULVC chain

A 32 bit ULV carry chain is implemented using 32 SDULVC circuits connected in a chain or NP domino fashion shown in Figure 22. Figure 24 shows the simulation response of a 32 bit ULV carry chain. The propagtion delay of this carry chain is 17ns. In order to compare the SDULVC to other carry gate topologies, a dual rail domino carry gate designed in a hybrid fashion, i.e., instead of utilizing conventional inverters at the output, the Static Differential ULV inverter presented in [14] and a conventional NP Domino Dual Rail carry is used. Compared to the hybrid dual rail domino carry (HDRDC) chain shown in the Figure 23 the SDULVC chain is almost 10× faster and compared to a Conventional Dual Rail Domino Carry (CDRDC) this is closer to 35×. These numbers are based on the propagation delay for the carry bit through the chain, which is 166ns for the hybrid dual rail domino carry and 636ns for the conventional dual rail domino carry, all at 300 mV.

The robustness of the SDULVC can be analyzed by looking at the simulation response shown in Figure 24b. The plot for the worst case delay scenario, i.e., A=1, B=0, C=0, exhibits that due to a delayed carry bit and the early arrival of inputs, A and B, a marginal transition at the output occurs. However, once the carry bit has arrived, the output shifts to its final value. Average transition at the output for a P-type and N-type SDULVC when waiting for the carry bit is between 70mV and 100mV. This can be seen as a problem for the noise margin and power consumption. The output manages to return to the right final value due to synchronisation of keeper signals with the input. Therefore, the issue of noise margin can be ignored by concluding that the final value can be read at the end of the evaluation phase.

Figure 25 shows the delay of an SDULVC chain compared

TABLE III. DIMENSIONS OF HYBRID DUAL RAIL DOMINO CARRY GATE

	Supply voltage variation	Width of dual rail domino evaluation transitor/Width of SDULVN evaluation transitor	Length of dual rail domino evaluation transitor/Length of SDULVN evaluation transitor	Width of dual rail domino precharge transitor/Width of SDULVN precharge transitor	Length of dual rail domino precharge transitor/Length of SDULVN precharge transitor
Size 1	270mv-400mv	4×	3.3×	1×	1×
Size 2	220mv-400mv	6.67×	8.3×	3.33×	35×

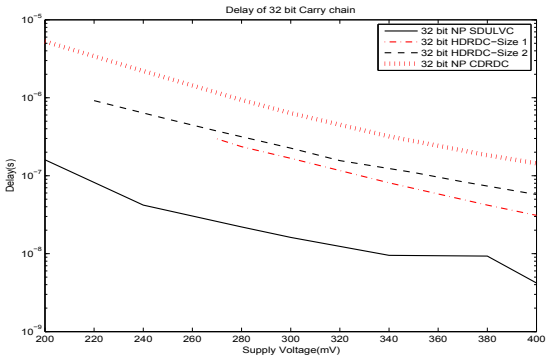


Fig. 25. Delay of 32 bit SDULVC and hybrid dual rail domino at varried supply voltage.

to an HDRDC and a CDRDC chain. Table III shows that the transistor size has to be increased in order to increase the ON current of the device [3] and be able to decrease the supply voltage for HDRDC. Table IV shows the minimum operating frequency required for the clock to simulate SDULVC, HDRDC and CDRDC at different supply voltages.

B. PDP and EDP of SDULVC chain

PDP charachteristics of a circuit highlights its efficiency with respect to power consumtion. A low PDP means a more energy efficient circuit. Although the ULV circuits presented in this paper are power hungry, it still manages to maintain its PDP at approximately the same level as conventional circuits where the power consumption is lower. The average power of the HDRDC and the SDULVC is $0.347\mu W$ and $1.28nW$ respectively at a supply voltage of 300 mV. This indicates that the power consumption of HDRDC is up to $3\times$ better than ULV circuits. However, at the same supply voltage the ULV circuit is $10\times$ faster than the HDRDC. Therefore, the ULV

TABLE IV. MINIMUM CLOCK OPERATING FREQUENCY FMIN REQUIRED BY THREE TOPOLOGIES

Supply Voltage (mV)	f_{min} for SDULVC (MHz)	f_{min} for HDRDC-Size 1 (MHz)	f_{min} for HDRDC-Size 2 (MHz)	f_{min} for CDRDC
200	1.6	-	-	0.08
220	-	-	-	-
240	3.125	-	-	0.217
250	-	-	0.83	-
270	-	1.66	1.225	-
280	6.25	-	-	0.5
300	8.33	2.3	2	0.769
320	-	-	2.27	-
340	16.66	5.5	3.33	1.562
380	21	10	5.55	2.5
400	23.8	60	7.692	3.33

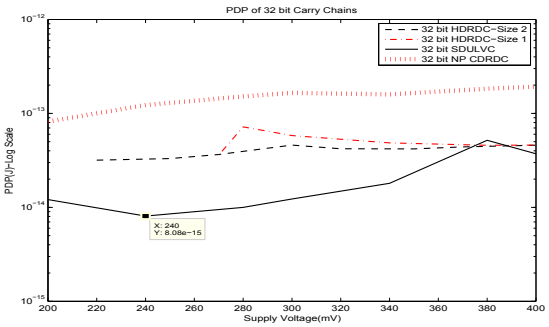


Fig. 26. PDP of 32 bit carry chains.

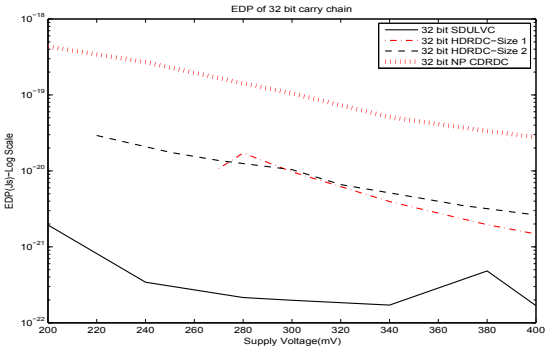


Fig. 27. EDP of 32 bit carry chains.

circiuts are still more energy efficient. Figure 26 shows PDP of three different 32 bit carry chain topologies at varied supply voltage. The minimum energy point of the 32 bit SDULVC carry chain is found at 240 mV.

Another important charachteristic of any circuit is EDP. It demonstrates enhanced speed of any circuit with respect to its energy effieciency. It is obvious that circuits with better propagation delay shall stand out in this characteristic. Figure 27 shows the EDP of three carry chains and the evident performance advantages of SDULVC circuits.

VIII. CONCLUSION PART 2

In this paper, a new ULV carry circuit has been presented and performance enhancements have been demonstrated. The ULV carry circuits are better than conventional topologies in both speed and energy efficiency, shown by comparing the SDULVC to the HDRDC and CDRDC circuit topologies. A credible conclusion is that a static differential dynamic ULV carry circuit is a favorable choice when speed and robustness at low voltages are important.

REFERENCES

[1] A. Majeed, H. Bechmann, and Y. Berg, "Novel High Speed and Robust Ultra Low Voltage CMOS NP Domino Carry gate," in *CENICS 2014, The Seventh International Conference on Advances in Circuits, Electronics and Micro-electronics*, 2014. [Online]. Available: http://www.thinkmind.org/index.php?view=article&articleid=cenics_2014_1_10_60004

[2] A. Chandrakasan, S. Sheng, and R. Brodersen, "Low-power cmos digital design," *Solid-State Circuits, IEEE Journal of*, vol. 27, no. 4, pp. 473 –484, Apr 1992.

[3] M. Alioto, "Ultra-low power vlsi circuit design demystified and explained: A tutorial," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 59, no. 1, pp. 3 –29, Jan. 2012.

[4] Y. Berg and O. Mirmotahari, "Ultra low-voltage and high speed dynamic and static cmos precharge logic," in *Faible Tension Faible Consommation (FTFC), 2012 IEEE*, June 2012, pp. 1 –4.

[5] S. Hanson, B. Zhai, M. Seok, B. Cline, K. Zhou, M. Singhal, M. Minuth, J. Olson, L. Nazhandali, T. Austin, D. Sylvester, and D. Blaauw, "Exploring variability and performance in a sub-200-mv processor," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 4, pp. 881 –891, April 2008.

[6] Y. Berg, D. Wisland, and T.-S. Lande, "Ultra low-voltage/low-power digital floating-gate circuits," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 46, no. 7, pp. 930–936, 1999.

[7] Y. Berg and O. Mirmotahari, "Static ultra low-voltage and high performance cmos nand and nor gates," *Rn*, vol. 1005, p. 2.

[8] N. Weste and D. Harris, *Integrated Circuit Design*. Pearson Education, Limited, 2010. [Online]. Available: http://books.google.no/books?id=gIAIQgAACAAJ

[9] M. Alioto and G. Palumbo, "Impact of supply voltage variations on full adder delay: Analysis and comparison," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 14, no. 12, pp. 1322–1335, 2006.

[10] ——, "Very high-speed carry computation based on mixed dynamic/transmission-gate full adders," in *Circuit Theory and Design, 2007. ECCTD 2007. 18th European Conference on*, 2007, pp. 799–802.

[11] Y. Berg and O. Mirmotahari, "Ultra low voltage and high speed cmos carry generate circuits," in *Circuit Theory and Design, 2009. ECCTD 2009. European Conference on*, 2009, pp. 69–72.

[12] Y. Berg, "Ultra low voltage static carry generate circuit," in *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*, 2010, pp. 1476–1479.

[13] Y. Berg, S. Aunet, O. Naess, O. Hagen, and M. Hovin, "A novel floating-gate multiple-valued cmos full-adder," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, vol. 1, 2002, pp. I–877–I–880 vol.1.

[14] Y. Berg and O. Mirmotahari, "Static differential ultra low-voltage domino cmos logic for high speed applications," *North atlantic university union: International Journal of Circuits, Systems and Signal Processing.*, pp. 269–274.