

Design of On-Chip GaN Transmitter for Wireless Communication

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Abstract— 5G standard is targeting much higher data rates as compared to existing wireless technologies to accommodate the ever-increasing demand for faster wireless applications. A transmitter is required to implement a 5G system. In this paper, we are presenting a 28 GHz novel monolithic transmitter architecture on GaN substrate that offers size, weight, area, power, and cost advantages. The transmitter contains a Yagi antenna, which consists of three directors, two drivers, a strip line feed, a substrate, and a ground plane. Optimization is obtained by modifying components design parameters. According to simulation results, the designed Yagi antenna has a compact size, and low loss at the selected frequency of 28 GHz. At this frequency, its return loss, gain, and beam width are -38 dB, 8.69 dB, and 57.2 degrees, respectively. The second component in the monolithic chain is a bandpass filter, which offers enhanced selectivity and stopband suppression on GaN substrate. The Bandpass filter has a minimum insertion loss of 0.6 dB at 28 GHz. The rejection level is higher than 10 dB in the stop band. Further, a collaborative simulation of 28 GHz mixer for upconversion with CLASS-E power amplifier with the integrated octature structure to achieve robust load insensitivity is presented. In this paper, to design high-efficiency PA, we implemented harmonic load pull at both the input and output of the active device to obtain optimum impedances at fundamental and second-harmonic frequencies. After an iterative process, the optimum input and output impedances are obtained. In addition, we also implemented a cascaded octature power cell structure. The proposed balanced PA achieves a saturated output power of 13.5 dBm and a maximum Power Added Efficiency of 55 %. It consumes 210 mW power. Each power cell is based on class-E. The circuit is implemented using GaN HEMT transistor taking an advantage of its high frequency and high power performance. The presented transmitter configuration is designed at 28 GHz for 5G Application on a GaN substrate with a thickness of 0.8 mm, a permittivity of 9.7, and loss tangent of 0.025.

Keywords—Yagi antenna; Filter; Mixer; Power amplifier; 5G.

I. INTRODUCTION

Fifth generation wireless network (5G) has become research focus since it could support the explosive growth of data traffic, massively interconnected devices, and new applications. It is expected that 5G will utilize spectrum at millimeter wave (mmw) frequencies to satisfy the demand for massive bandwidth since the spectrum resources in the lower frequency bands are running out. mmw frequency is attractive because of the rich spectrum resources and advantages of size, weight, and power. Further, there are several motivations to use mmw frequencies in radio links such as availability of

wider bandwidth, relatively narrow beam widths, better spatial resolution and small wavelength allowing modest size antennas to have a small beam width. Resources have been invested to develop prototype millimeter wave 5G mobile communication systems, especially for frequency band such as 28 GHz [1]. Therefore, 27.5 to the 29.5 GHz band is a strong candidate for the new 5G radio interface and much of the research undertaken to date has considered this band. For example, Samsung Electronics has built a prototype system including beamforming antenna that works at 28 GHz [2][3]. However, to our knowledge single chip transmitter on gallium nitride (GaN) does not exist for the 5G application.

An overview of the architecture and components for our transmitter module on a GaN chip is shown in Fig. 1. The Integrated chip consists of a chain of various individual components such as yagi antenna, power amplifier, bandpass filter, upconverter, mixer and matching circuitry. The presented transmitter configuration is designed on a GaN substrate with a thickness of 0.8 mm, a permittivity (ϵ_r) of 9.7, and loss tangent ($\tan\delta$) of 0.025. The goal is to ultimately fabricate the proposed transmitter module on GaN substrate.

The Yagi antenna is designed using High-Frequency Structure Simulator (HFSS) simulation software. Rest of the blocks of the transmitter, bandpass filter (BPF), Mixer, Power amplifier (PA), and matching network circuitry are designed using Advanced Design System (ADS) simulation software. The proposed transmitter design and results are mentioned in Section II and concluded in Section III.

II. DESIGN AND RESULT & DISCUSSION OF TRANSMITTER MODULE ON GAN CHIP

Designing of the transmitter blocks are mentioned here.

A. Yagi Antenna

Yagi antenna was proposed by researchers from Japan [4][5] usually for radio application [6]. Such antenna was developed for X-band, Ku-band, and K-band, etc. Generally, a design of Yagi antenna places a driver and director's elements on one side of a printed circuit board (PCB) and places a reflector on the reverse side. A driver is utilized for radiating electromagnetic wave whilst directors and a reflector is utilized to focus the electromagnetic wave radiation from its driver. But, the design of Yagi antenna is more challenging if it is being designed at 28 GHz on GaN substrate instead of PCB.

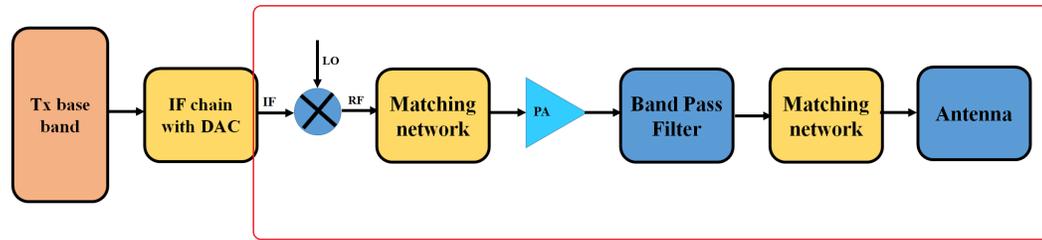
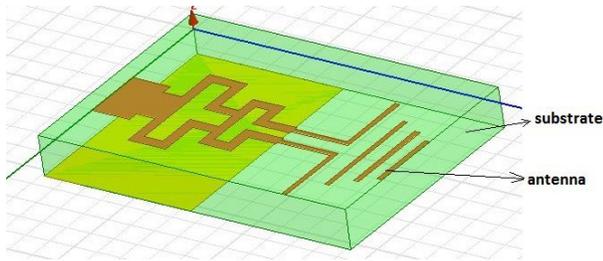
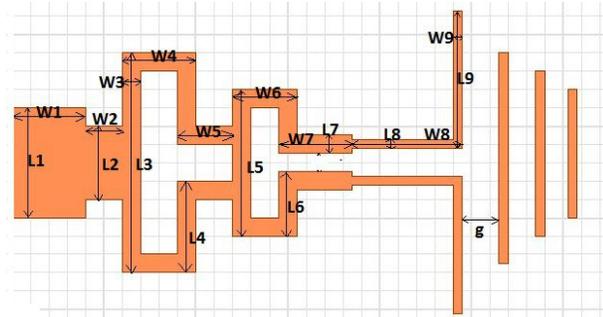


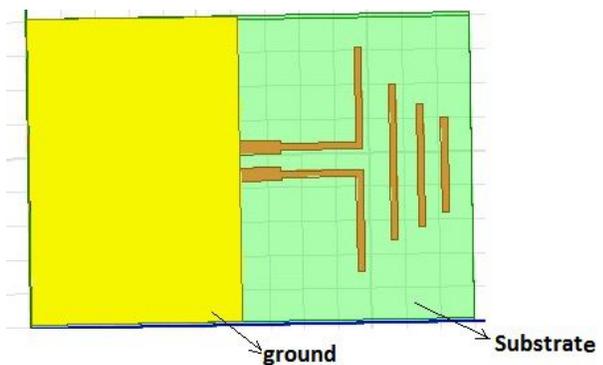
Figure 1. Transmitter architecture for 5G application



(a)



(b)



(c)

Figure 2. (a) 3D view of Antenna in HFSS (b) Dimensions of yagiguda antenna (c) Bottom view of yagiguda antenna

design of the proposed Yagi antenna is shown in Fig. 2. It is composed of three directors, two drivers, a strip line for feed and a reflector. This antenna can be configured in multiple input and multiple output (MIMO) formats if needed. The antenna is made from gold with a thickness of 0.035 mm and electric conductivity of 4.1×10^7 Siemens/m considering GaN as substrate.

In order to match antenna impedance with another device, the impedance was optimized for 50Ω . To fulfill such requirement, its feed- width was set to be 1.8 mm. Details of the Yagi antenna design parameters that showed best performance is shown in Table I.

TABLE I. DIMENSIONS OF PROPOSED ANTENNA

L1	L2	L3	L4	L5	L6	L7	L8	L9	g
1.8	0.9	2.5	1.2	2	0.8	0.5	0.3	2	0.1
W1	W2	W3	W4	W5	W6	W7	W8	W9	
1.5	0.7	0.5	1.5	0.5	1.5	1.8	2.5	0.3	

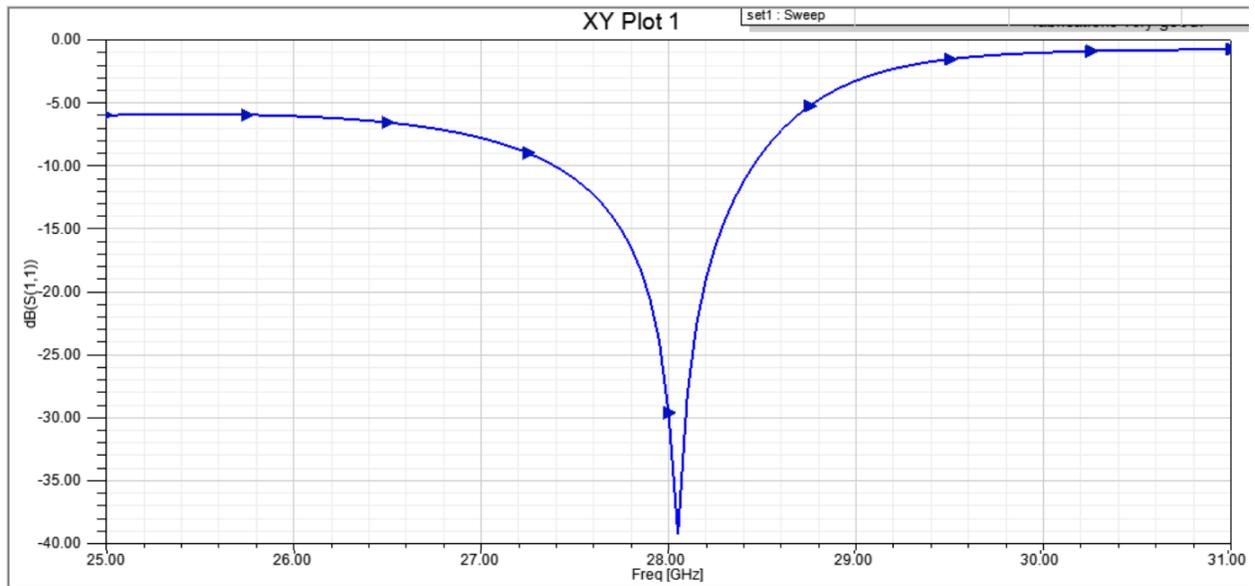
Fig. 3a shows simulated return loss of -38 dB for 27.4 GHz to 28.4 GHz with a center frequency of 28 GHz. Fig. 3b shows simulated radiation pattern, which is unidirectional with the main lobe at 342 degrees. At its main lobe, the gain is 8.69 dB. Its beam width is 57.2 degree, which its half power beam width occurring at -26.44 degree and 30.7 degrees. The front to back ratio of the antenna is nearly 17.4 dB. The antenna 3D radiation pattern and voltage standing wave ratio (VSWR) are shown in Fig. 3c and Fig. 3d, respectively. Usually for a good antenna VSWR should be below 2. Our simulation shows that during the passband frequency antennas VSWR is below 1.8. The simulated results of the antenna are listed in Table II.

TABLE II. ANTENNA RESULTS

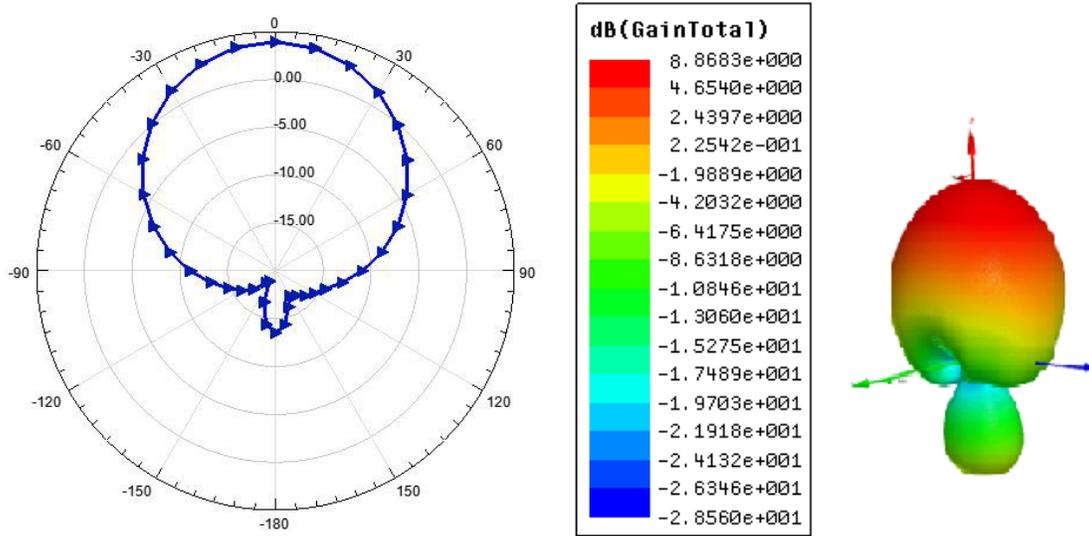
Content		Units	
Antenna type			Yagi guda
Antenna array size (L*W)		mm*mm	8*12
Peak Directivity		dB	8.9
Antenna bandwidth		GHz	27.4-28.4
Radiated power		W	0.8
Accepted power		W	0.9
Radiation Efficiency	At 28 GHz	%	96
VSWR	At 28 GHz	GHz	<1
GaN substrate details			
Assumed during simulation	Thickness	mm	0.8
	Er		9.7
	Tan D		0

In this paper, we present the design of novel structure Yagi antenna, which shows good radiation efficiency and gain. The

A comparison of performances of proposed work antenna with previously published works is highlighted in Table III.

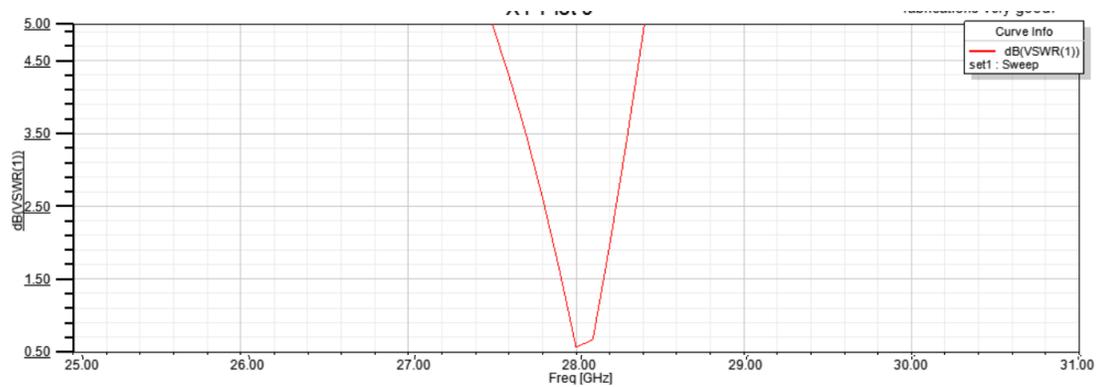


(a)



(b)

(c)



(d)

Figure 3. (a) S11 response or return loss of antenna (b) Radiation ptttern of antenna (c) 3D gain of antenn (d) VSWR of the antenna

TABLE III. DESIGN SPECIFICATION COMPARISON OF PROPOSED WORK AND PREVIOUSLY PUBLISHED WORKS

Key Parameter	Contents	Units	Proposed	Published		
				[7] 2017	[8] 2017	[9] 2018
Antenna	Year		2018	26.43 to 29.32	27.93 to 28.33	27.9 and 28.5
	Bandwidth	GHz	27.4-28.4	26.43 to 29.32	27.93 to 28.33	27.9 and 28.5
	S11	dB	-40	-35	-14	-22
	Gain	dB	8.69	12.5	2.03	4.5
	Efficiency	%	96	68	73.4	50

TABLE IV. DESIGN SPECIFICATION COMPARISON OF PROPOSED WORK AND PREVIOUSLY PUBLISHED WORKS

Key parameter	Contents	Units	Proposed	Published		
				[10] 2016	[11] 2015	[12] 2015
Band Pass Filter	Year		2018	58 to 62	38 to 42	21.4 to 38.9
	Bandwidth	GHz	27.6 to 29.2	58 to 62	38 to 42	21.4 to 38.9
	S11	dB	-40	-20	-40	-30
	S21	dB	0.6	0.008	0.97	1

Return loss and efficiency of antenna are better than recently published works.

B. Bandpass Filter Design

Filters are an essential part of wireless communications systems as they are required to suppress undesired signals in the transceiver pass-band. The size, weight, cost, and loss of such filters must be kept as low as possible. Currently, separate filters (low pass, band pass, and high pass) are used to suppress unwanted signals depending upon system requirements and they are designed and integrated separately. Hence, there is a critical need for a multifunction filter, which can be integrated on-chip to support multiband operation [13] of a transceiver.

resonators are implemented on two-layer GaN substrate, which has relatively small sizes and good selectivity.

The dimensions of the BPF filter are listed in Table V.

TABLE V. BPF DIMENSIONS

L1	L2	L3	L4	L5	L6	L7	L8	L9	g
8.8	13.5	5	6	2	5	4	5	6.5	0.5
W1	W2	W3	W4	W5	W6	W7	W8	W9	
3	2.2	3.5	1.5	1	1	0.6	3.5	0.1	

Fig. 5 shows the simulated results of the designed bandpass filter. The 3 dB bandwidth is from 27.6 GHz to 29.2 GHz. This filter has a minimum insertion loss of 0.6 dB at 28 GHz. The rejection level is higher than 10 dB in the stop band. The return loss of bandpass filter is more than -40 dB at 28 GHz.

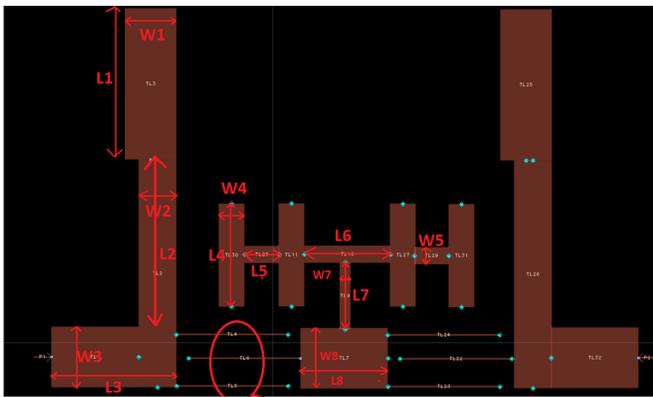


Figure 4. Band pass filter structure with dimensions

In this paper, the design of a core circuit using a microstrip line has been conceived and designed as shown in Fig. 4. Small size, low cost, and good performance multifunction filters are the with high selectivity and good stopband performances are extensively studied [14]. On the other hand, the GaN substrate has attractive characteristics, such as wide frequency range, static dielectric constant, low thermal expansion coefficient and very low water absorption [15]. Moreover, the combination of excellent electrical performance, multilayer integration capabilities and low cost makes GaN extremely attractive for designing radio frequency (RF) circuits with high integration [15]. In this paper, a bandpass filter based on broadside coupling H-shape resonators and a half wavelength

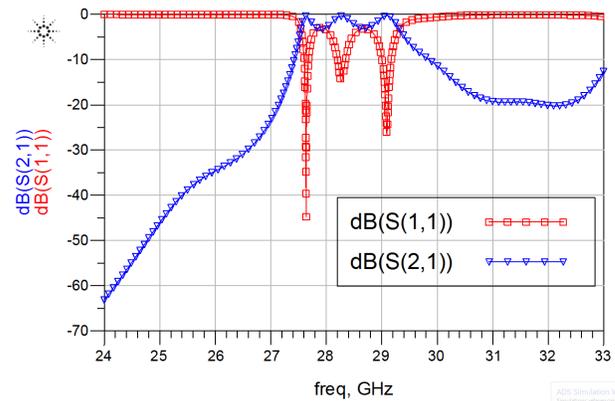


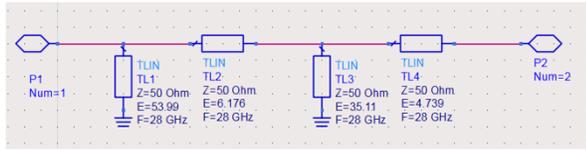
Figure 5. S11 response of antenna

A comparison of performances of proposed work BPF with previously published works is highlighted in Table IV. Return loss is better than recently published works.

C. Impedance Matching Network

At 28 GHz frequency, the reflected power occurs when the load impedance is not matched to the characteristic impedance of source (mixer) and load (PA). Impedance matching using the passive network is critical in the design of microwave circuits to achieve maximum power transfer, minimum reflection, and adequate harmonic rejection. Traditionally spiral inductors are

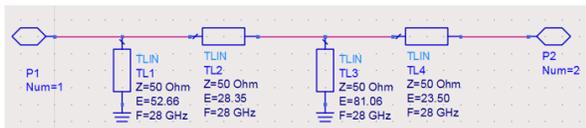
preferred instead of resistors and transmission lines to enhance the thermal noise performance; however, they cannot be used at high frequency because of the self-resonance and stray impedances. In addition, they also occupy large on chip space.



(a)



(b)



(c)

Figure 6. : (a) The topology of the matching networks between the filter and Rectifier (b) Optimization of transducer gain (c) The topology of the matching networks between the Rectifier and load

In order to overcome such problems, we adopted a new design strategy in this paper. The proposed approach is based on closed-form and recursive relationships [16]. The proposed matching network approach is based on a closed analysis, allowing the direct synthesis of multi-frequency matching network through micro-strip lines. Through Smith chart, we can get a matching network at a certain frequency easily, maybe an L or Π network is enough.

Theoretical approach: In a resonance circuit, we define the loads Q value

$$Q_L = \frac{f_0}{BW} \quad (1)$$

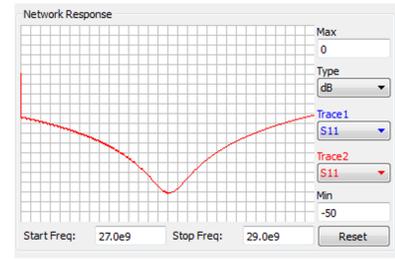
f_0 is the resonance frequency; BW is the bandwidth. There is equal serial input impedance at every circuit node of the matching networks.

$$Z_{in} = R_s + jX_s \quad (2)$$

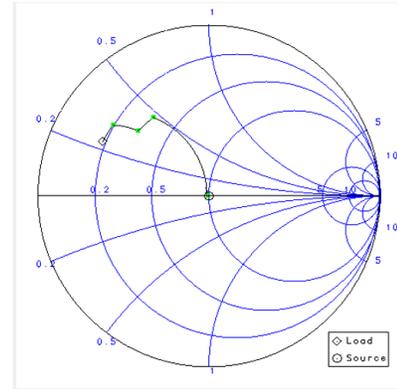
The Q value of every circuit node is:

$$Q_n = \frac{|X_s|}{R_s} \quad (3)$$

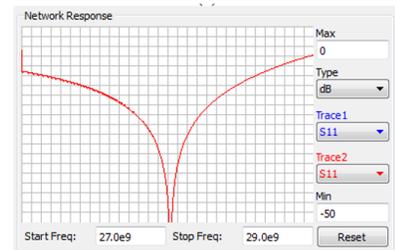
In the Smith chart, the equal Q_n curve is a cycle, the center coordinate is $(0, -1/Q_n)$, the radius is



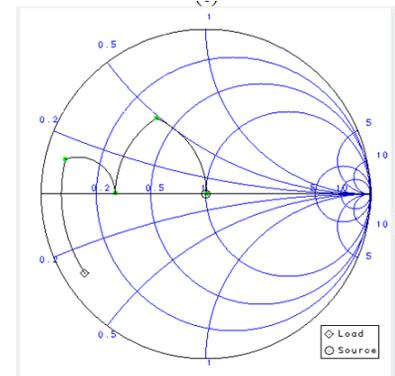
(a)



(b)



(c)



(d)

Figure 7. : (a) Network Response of impedance Schematic of Fig. 6a (b) Smith Chart Response-impedance matching of Fig. 6a. (c) Network Response of impedance Schematic of Fig. 6c (d) Smith Chart Response-impedance matching of Fig. 6c.

$$\sqrt{\left(1 + \frac{1}{Q_n^2}\right)} \quad (4)$$

The value of Q_L is decided by the value of Q_n . Therefore, in order to increase the bandwidth, we should reduce the value of Q_n . While the least Q_n is the maximum of the source and load impedances Q value. When utilizing the Smith chart to design matching networks at the center frequency, the the next steps should be followed:

- 1) Find out the output impedance Z_{out} of the previous stage transistor and the input impedance Z_{in} of next stage transistor.
- 2) Find out the points of Z_{out} , Z_{in} in the Smith chart.
- 3) Describe the maximum equal Q curve Q_{max} from the points of Z_{out} , Z_{in} .
- 4) In the extension of the Smith chart constructed by Q_{max} , add appropriate micro strips and capacitances to make Z_{out} and Z_{in} conjugate match.

Then consider the network composed of microstrips as the initial matching network. We designed such matching network using ADS. This network is designed to operate at 28 GHz frequency with the normalized impedance of 50Ω . Where Z_S is antenna output impedance, Z_L is Filter input impedance.

We calculated the stub values mentioned in Fig. 6 using ADS. Fig. 6 shows the objective function to optimize the whole matching networks. During 27 GHz to 29 GHz, the maximum transducer gain limit to 64 dB and the minimum transducer gain is 63 dB. As a result, we can get a good transducer curve, whose flatness is less than 0.2 dB at the desired frequency of 28 GHz.

Traditionally Network Response is calculated to check loss value of circuit. So, we plotted S_{11} to find the loss of the network schematic, the S_{11} value at 28 GHz is lower than -10 dB. To investigate circuit stability and perfect match we plotted impedance (Fig. 7) on Smith chart as shown in Fig. 7.

D. Mixer Design

Transmit Signal coming from baseband is almost at direct current (DC), hence it must be upconverted to high frequency at which the antenna is working. In order to do that signal must be up-converted using mmw mixer. Doubly-balanced Mixers (DBM) are usually the desirable mixer because of their superior suppression of spurious mixing products and good port-to-port isolation [2]. The mixers based on the ring or star configurations balun were used widely, but most of them are designed for narrow-band only. An ultra-wideband balanced microstrip balun was reported [17][18], but this type of balun was difficult to fabricate. A 28 GHz mixer based on the Marchand balun was fabricated in 0.15m GaAs PHEMT technology, similar to our proposed design in GaN technology.

In this paper, a 28 GHz doubly-balance mixer based on the [19] Marchand balun in the 27 GHz to 30 GHz RF/LO range and DC to 5 GHz IF is presented. The collaborative simulation of HFSS and ADS has been adopted in mixer design, the balun in LO port and RF port are simulated by the full-wave the electromagnetic simulator in HFSS, then the S parameter data of the balun are exported to the mixer circuit in ADS. The mixer offers about 10 dB typical conversion loss, high gain compression, higher than 20 dB LO-to-RF isolations and about 10 dB return loss across 27 GHz to 30 GHz.

1) *The Balun Design:* The balun was simulated by using Ansoft HFSS and Agilent ADS. The Marchand balun was compensated by two open-circuited stubs at the output ports,

the coupled line model in the circuit initially was used to predict the performance, and then simulated by using the full-wave electromagnetic simulator to improve the accuracy of the simulation finally. The 3D structure of the balun used in the mixer was drawn by HFSS and shown in Fig. 8, which is designed for GaN substrate with thickness 0.8 mm and dielectric constant 9.7. 1 is the input port and 2 3 are output ports. Impedances of three ports are all set to be 50Ω and the microstrip line width is 0.25 mm, and l. w2 and w3 stand for the length the width and the gap width of the microstrip lines, the hole is metallization and connected to ground. The Marchand balun is simulated by optimizing w2 and w3.

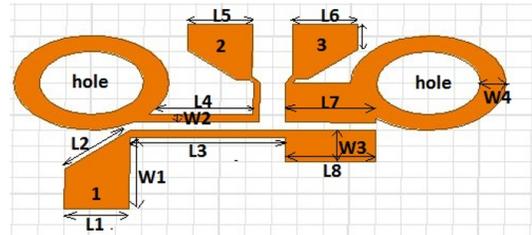


Figure 8. Structure of mixers balun

Dimensions of mixers balun are mentioned in Table VI.

TABLE VI. DIMENSIONS OF MIXERS BALUN STRUCTURE

L1	L2	L3	L4	L5	L6	L7	L8
1.2	1.5	2.5	1.8	1.2	1.2	1.4	1.4
W1	W2	W3	W4				
1.2	0.2	0.5	0.3				

2) *The Mixer Design:* Then the terminal S parameter data of the balun in HFSS are exported to the mixer circuit in ADS in Fig. 9, the three ports network are set up to substitute the balun. RF port and LO port is power source port, the IF port is load port, all the port is set to 50Ω . Two gold lines are set to near the real condition, the line is set to 5 mm length and the diameter is 0.1 mm. The capacitances are used in LO port to make the minimal frequency of the IF port extend to DC. $C1=C2=0.5 \text{ pF}$. The simulated result of the mixer circuit conversion gain was obtained using the harmonic balance method in Fig. 10. The type conversion gain is about 9.3 dB.

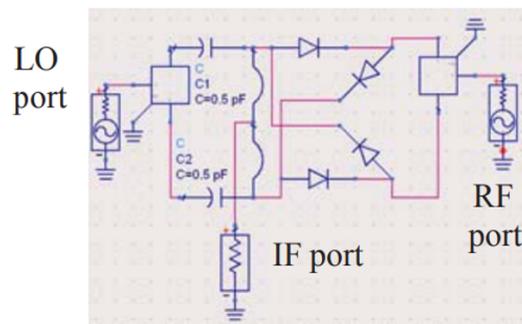


Figure 9. Double balanced mixer circuit in ADS

Fig.11 shows the results of the conversion loss and the isolation are obtained when the LO power is about 12 dBm

TABLE VII. DESIGN SPECIFICATION COMPARISON OF PROPOSED WORK AND PREVIOUSLY PUBLISHED WORKS

Key Parameter	Contents	Units	Proposed	Published		
Mixer	Year		2018	[20] 2013	[21] 2017	[22] 2017
	Frequency	GHz	28	130	60	2.4
	Conversion Gain	dB	9.3	3	4	10

and IF output is at 400 MHz across the bandwidth from 27 GHz to 30 GHz.

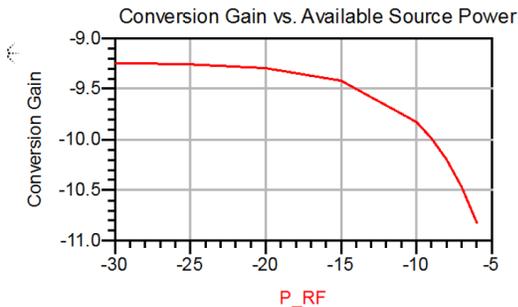


Figure 10. Conversion Gain vs available source power

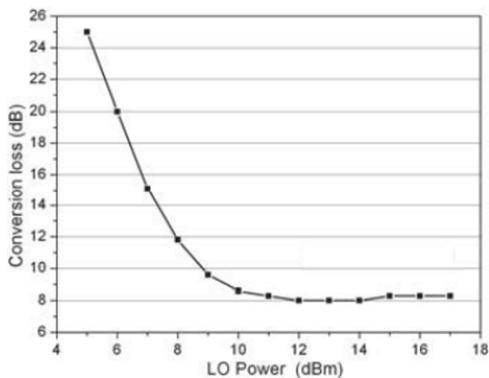


Figure 11. Conversion loss (dB)

A comparison of performances of proposed work Mixer with previously published works is highlighted in Table VII. Conversion gain of the mixer is better than recently published works.

E. Power Amplifier Design

For wireless communication systems, power amplifiers (PAs) with high efficiency is critical as they consume the majority of the power of the systems and closely related to the thermal problem. As a result, many categories of high-efficiency PAs have been widely studied in recent years [23][24]. The Class-E amplifier is well known for its high efficiency and simple structure. However, the very high breakdown voltage of three times the dc supply voltage of the transistor is required [25]. Moreover, the inherent output capacitor of a transistor deteriorates the performance of a Class-E amplifier at high frequency. To address the above problems, the Class-E amplifier was designed by modifying the device output impedances at odd and even harmonics, so as to shape the output voltage and current that minimize the overlap to achieve

high efficiency [26]. However, since the openshort impedance is derived in the infinite harmonic condition, the matching network of a Class-E amplifier should be able to tune high-order (beyond third order [27]) harmonics, which make the circuit implementation more complex.

In this paper, a simple method of designing high-efficiency PA is presented. Compared with other works, this method is easier to design harmonic tuned PA and thus achieves relatively high efficiency with fewer harmonics to control. The simulated results indicate a high-efficiency Class-E PA is realized with 55% PAE and 13.5 dBm output power at 28 GHz.

However, the challenge of the MMW PA design is to deliver maximum output power with a maximum Power Added Efficiency (PAE) and high linearity [28][29]. For this purpose, to achieve high efficiency, we have implemented two techniques. Technique one is harmonic load pull conducted at both the input and output of the active device to obtain optimum impedances at fundamental and second-harmonic frequencies. After an iterative process, the optimum input and output impedances are obtained. Technique two is cascaded octature power cells structure is implemented. The presented circuit is implemented in GaN HEMT technology (as shown in Fig. 12) taking the advantage of high-frequency performance and high power performance [15].

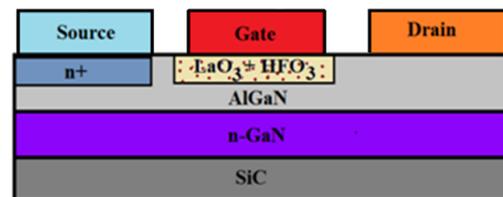


Figure 12. GaN HEMT transistor structure

1) *Design Process*: The design of each PA commenced with the selection of the transistor size and bias. Increasing the total gate width of the selected transistor also increases the available RF output power. However, the higher parasitic of the physically larger transistor results in a reduction in available gain. The proven design approach to address this is to use multiple power-combined transistors. To achieve the target output power, a total of eight stages were power-combined in the output stage. This output stage was driven by a pair of devices, and this, in turn, was driven by an input stage realized using a single transistor. The transistor sizes in each stage needed to be identical, and the basic power-combining topology needed to be similar.

The individual PA structure is shown in Fig. 13 is composed of three series transmission lines with one parallel open-circuit stub located between the first two lines are used as the impedance matching circuit, which is a simplified method of the distributed multi-frequency matching approach, as in-

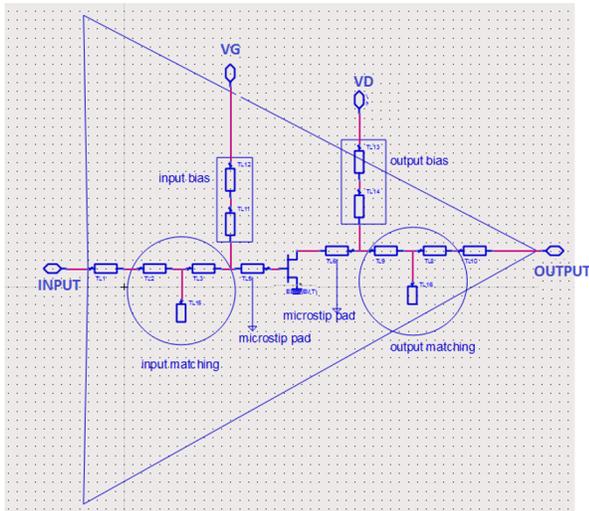


Figure 13. Single stage PA design

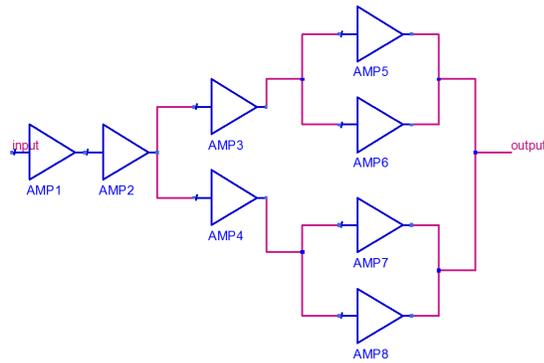


Figure 14. Octature structure PA design

roduced previously [30]. The single transmission line before the open stub is used to tune the impedance of the second harmonic, while the two series transmission lines after the open stub are used to tune the impedance of the fundamental mode. Therefore, optimum impedance control at fundamental and second-harmonic frequencies can be realized simultaneously.

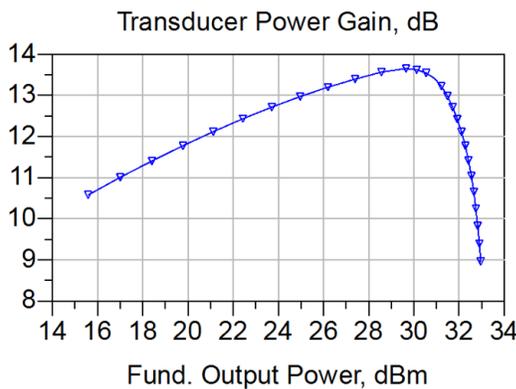


Figure 15. Transducer power gain of PA for single stage

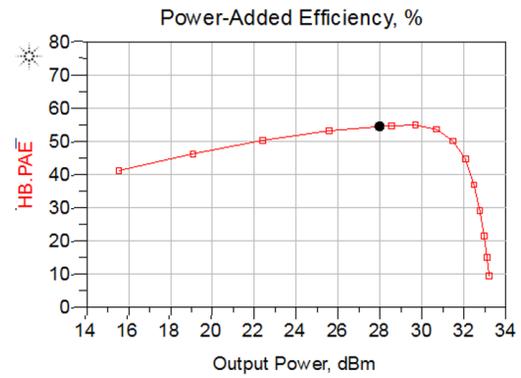


Figure 16. Power added efficiency of PA

Fig. 15 shows the simulated power gain plots of the PA. The PA response is clearly evident at the 28 GHz band in blue. The amplifier shows good input and output return loss in each band and has a small signal gain of 13.5 dB. The simulated large-signal performance is plotted in Fig. 16 and 17. As with the small-signal case, the performance of the amplifier operating in the 28 GHz band is plotted in red. Power added efficiency is around 55 %. The balanced topology offers a very good VSWR robustness. DC power consumption of PA is plotted in Fig. 18; our PA consumes 210 milli watts at 28 GHz.

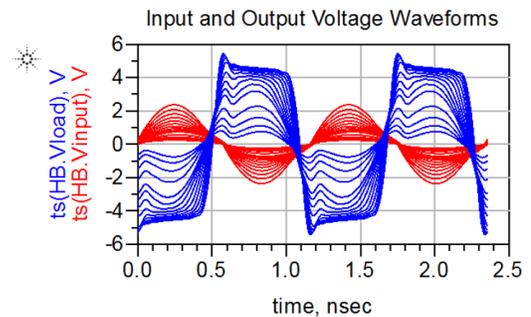


Figure 17. input and output waveforms of PA

A comparison of performances of proposed work power amplifier with previously published works is highlighted in Table VIII. Power efficiency of the power amplifier is better

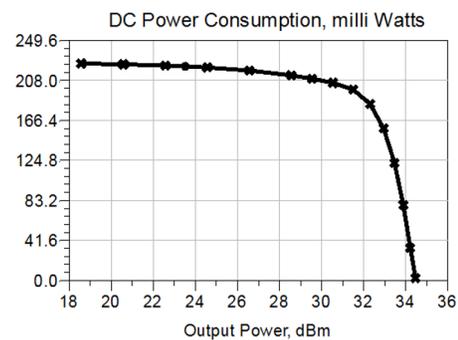


Figure 18. DC Power consumption, milli-watts

TABLE VIII. DESIGN SPECIFICATION COMPARISON OF PROPOSED WORK AND PREVIOUSLY PUBLISHED WORKS

Key Parameter	Contents	Units	Proposed	Published		
				[31] 2018	[32] 2017	[33] 2017
Power Amplifier	year		2018	[31] 2018	[32] 2017	[33] 2017
	Frequency	GHz	28	28	29-57	37-40
	Efficiency	%	55	40	24.2	28

than recently published works.

F. End to End Module Performance

To investigate the loss of proposed the transmitter architecture, we have simulated S11 of transmitter module chain (with Yagi antenna, bandpass filter, mixer, matching network and power amplifier) in ADS. The results are shown in Fig. 19. We plotted S11 to find the loss of the whole module and the S11 value at 28 GHz is lower than -30 dB, which is excellent.

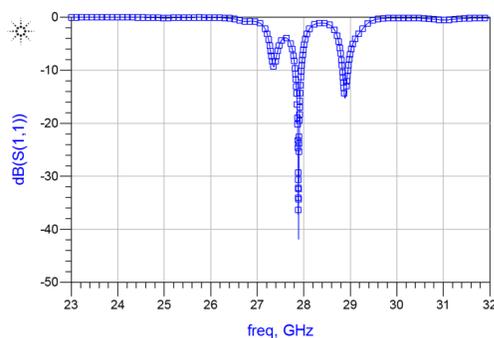


Figure 19. Simulated transmitter architecture end to end S11 response

III. CONCLUSION

The design of a novel transmitter module on a single a chip using GaN/Si as the substrate is presented in this paper. The transmitter module consists of Yagi antenna, bandpass filter, impedance matching network, upconversion mixer, and power amplifier. We investigated innovative designs for the transmitter components with potential for integration on a GaN substrate. To validate our designs, we selected 28 GHz but module design can be easily scaled to higher millimeter wave frequencies such as 60 GHz for the 5G system. Designed transmitter module shows loss of less than -10 dB at 28 GHz, which can be further improved with design refinement. To our knowledge, this is first reported the design of monolithic transmitter module on GaN chip. Our proposed module will offer significant SWAP-C advantages.

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