



CENICS 2013

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CENICS 2013 Editors

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CENICS 2013

Foreword

The Sixth International Conference on Advances in Circuits, Electronics and Micro-electronics [CENICS 2013], held between August 25-31, 2013 in Barcelona, Spain, continued a series of events initiated in 2008, capturing the advances on special circuits, electronics, and micro-electronics on both theory and practice, from fabrication to applications using these special circuits and systems. The topics cover fundamentals of design and implementation, techniques for deployment in various applications, and advances in signal processing.

Innovations in special circuits, electronics and micro-electronics are the key support for a large spectrum of applications. The conference is focusing on several complementary aspects and targets the advances in each on it: signal processing and electronics for high speed processing, micro- and nano-electronics, special electronics for implantable and wearable devices, sensor related electronics focusing on low energy consumption, and special applications domains of telemedicine and ehealth, bio-systems, navigation systems, automotive systems, home-oriented electronics, bio-systems, etc. These applications led to special design and implementation techniques, reconfigurable and self-reconfigurable devices, and require particular methodologies to be integrated on already existing Internet-based communications and applications. Special care is required for particular devices intended to work directly with human body (implantable, wearable, eHealth), or in a human-close environment (telemedicine, house-oriented, navigation, automotive). The mini-size required by such devices confronted the scientists with special signal processing requirements.

We take here the opportunity to warmly thank all the members of the CENICS 2013 Technical Program Committee, as well as the numerous reviewers. The creation of such a high quality conference program would not have been possible without their involvement. We also kindly thank all the authors who dedicated much of their time and efforts to contribute to CENICS 2013. We truly believe that, thanks to all these efforts, the final conference program consisted of top quality contributions.

Also, this event could not have been a reality without the support of many individuals, organizations, and sponsors. We are grateful to the members of the CENICS 2013 organizing committee for their help in handling the logistics and for their work to make this professional meeting a success.

We hope that CENICS 2013 was a successful international forum for the exchange of ideas and results between academia and industry and for the promotion of progress in the field of circuits, electronics and micro-electronics.

We hope Barcelona provided a pleasant environment during the conference and everyone saved some time for exploring this beautiful city.

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High Speed and Ultra Low-Voltage CMOS Carry Propagation Chain using Floating-Gate Transistors

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Abstract—Ultra low-voltage (ULV) CMOS logic for high-performance applications is presented. By applying floating capacitors we can increase the current level of MOS transistors for supply voltages below $500mV$. The current level of the transistors may be increased by a factor 40 for supply voltages below $0.3V$. Simple NAND gates are presented using different topologies. The NAND gates are exploited to provide a high-speed and ultra low-voltage serial carry chain. Compared to conventional serial CMOS carry gates the delay is reduced by a factor 10 or more. Simulated data are based on *SpectreS* simulator provided by *Cadence* and are valid for 90nm TSMC CMOS process.

Keywords-CMOS; Low-Voltage; Carry; High-Speed; Floating-Gate; Pass Transistors.

I. INTRODUCTION

The demand for high-speed digital circuits is ever increasing. At the same time the supply voltages in modern CMOS processes are reduced in order to prevent transistor failure due to short channel effects. The low supply voltage is a challenge for high-speed circuit design. With the emergence of sensor and biomedical applications that require ultra low energy [1], [2], we have to adequately address design optimization near the minimum-energy point. It has long been established that for most logic families the minimum-energy point occurs in the subthreshold operational region of the MOS transistors and that the value of the minimum energy is set by leakage current.

Energy-efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. The general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of high-speed circuits. The supply voltage region addressed in this paper is between $200mV$ and $400mV$. In this region traditional CMOS logic design is hampered with subthreshold current which both reduces the circuit speed and robustness. In the approach presented in this paper the main transistors are operating above the threshold voltage

for ultra low supply voltages. For a supply voltage equal to $300mV$ the delay of the proposed carry gates is reduced to less than 10% of a conventional CMOS carry gate while the noise margin is increased due to an enhanced current level. The delay variation is reduced accordingly due to large driving currents. The energy required to drive the gates are comparable to conventional CMOS [3].

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. Thus, taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay is of great interest for the implementation of modern digital systems. Arithmetic circuits, like adders and multipliers, are also one of the basic components in the design of communication circuits.

The ultra low-voltage circuits presented in this paper are derived from digital floating-gate circuits [4]. In Section II, we introduce ultra low-voltage semi-floating-gate logic and compare the performance to conventional, i.e., complementary CMOS. ULV NP domino inverters are described and the potential delay reduction and increased performance in terms of minimum-energy-point (MEP) is presented. In Section III, we present novel ULV NAND and AND gates using enhanced pass transistors. Different ultra low-voltage carry gates are presented in Section IV. The high-speed ULV carry gates can be used in simple serial adders to reduce the complexity of parallel conventional CMOS adders for supply voltages below $500mV$.

II. ULTRA-LOW-VOLTAGE SEMI-FLOATING-GATE LOGIC

The ULV logic styles presented in this paper are related to the ULV domino logic style presented in [5]. The main purpose of the ULV logic style is to increase the current level for low supply voltages without increasing the transistor widths. We may increase the current level compared to complementary CMOS using different initialization voltages to the gates and applying capacitive inputs. The extra loads represented by the floating capacitors are less than extra load given by increased transistor widths. The capacitive inputs

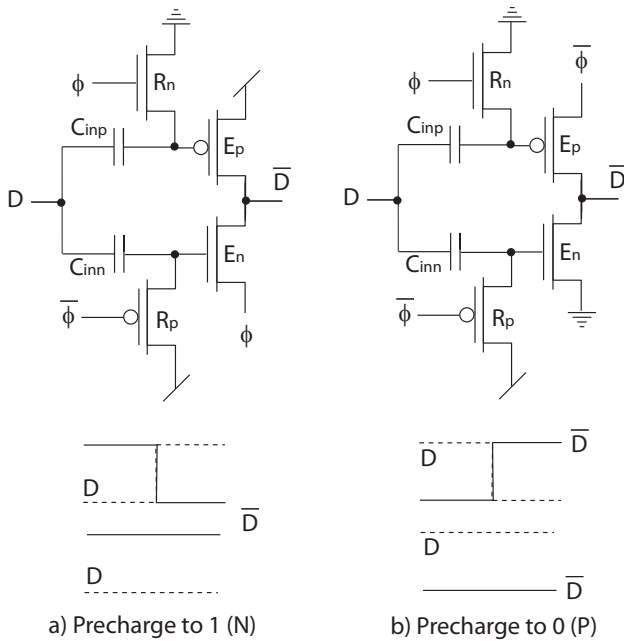


Figure 1: ULV domino inverters.

lower the delay through increased transconductance while increased transistor widths only reduce parasitic delay. Furthermore, the accuracy of the capacitor values are not critical and the process variations and temperature will only have a significant impact on the transistor currents through the high relative transconductance in the subthreshold region. The ULV logic styles may be used in critical sub circuits where high speed and low supply voltage is required. The ULV logic styles may be used together with more conventional CMOS logic and will require a specialized CMOS process. The floating capacitors can be either poly-poly, metal-metal or MOS parasitics.

The simple dynamic edge and level ULV inverters [5] are shown in Figure 1. Apply a clock signal to power the inverter, i.e., either ϕ to E_n to and V_{DD} to E_p , or $\bar{\phi}$ to E_p and GND to E_n and precharge to 1 or 0 respectively. The gate resembles NP domino logic. In order to hold the precharged value until an input transition arrives the E transistor connected to a supply voltage is made stronger than the other E transistor. The function of the inverter can be described as $\bar{O} = \bar{A}D$

The different ULV logic styles are defined by the applied terminal inputs as shown in Table I. ΔV is the output voltage swing. The simple model for the noise margin NM' is given by the ratio of the ON current and the OFF current. The capacitive division factor, $\frac{C_{in}}{C_T}$ where C_T is the total capacitance seen by a floating gate is assumed to be 0.5. The delay is relative to a standard complementary CMOS inverter. The ON and OFF currents of a complementary CMOS inverter is given by the effective gate source voltages V_{DD} and $0V$ respectively. Assuming $\frac{C_{in}}{C_T} = 0.5$ where C_T is

the total capacitance seen by a floating gate, we may estimate the delay, dynamic and static power and noise margins of the different ULV logic styles relative to a complementary CMOS inverter.

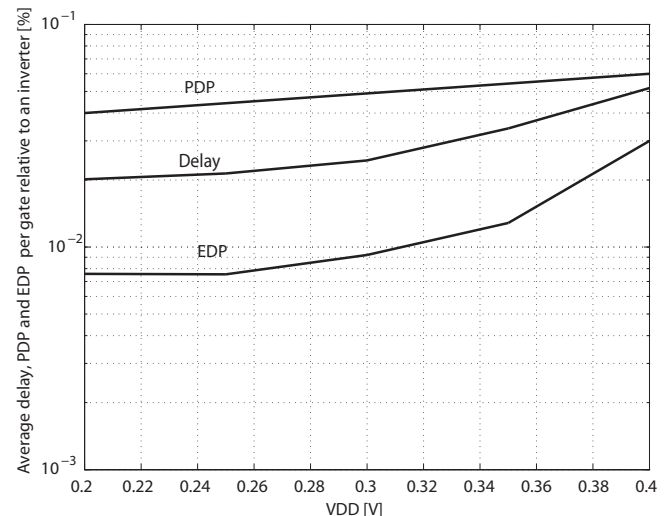


Figure 2: Performance.

The ULV domino inverters can exploited to improve speed for ultra low supply voltages. Relative delay, Power-Delay-Product (PDP) and Energy-Delay-Product (EDP) for ULV inverter compared to complementary CMOS is shown in Figure 2, the delay for supply voltages below 0.4V can be reduced to less than 5%.

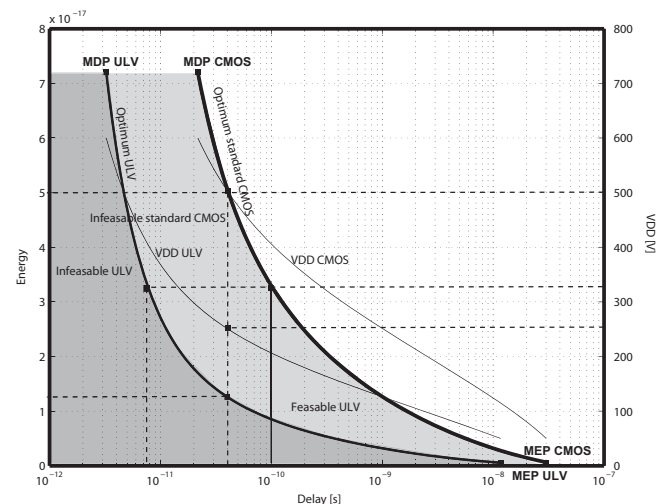


Figure 3: Energy delay trade-off, complementary CMOS and ULV.

The optimum energy-delay trade-off in standard CMOS logic, shown in Figure 3, is traditionally close to the minimum-delay point (MDP). The region left of the optimum energy-delay curve is not feasible for conventional or standard CMOS logic. By applying a current boost provided

Table I: ULV LOGIC STYLES

ΔV	E_p	E_n	$V_{gs} I_{ON}$	$V_{gs} I_{OFF}$	NM'	Relative delay	Style	Comment
$\pm \frac{V_{DD}}{2}$	$\bar{\phi}$	ϕ	$\frac{5V_{DD}}{4}$	$\frac{3V_{DD}}{4}$	$\frac{V_{DD}}{2}$	$\approx 10\%$	DU	Dynamic
V_{DD}	$\bar{\phi}$	GND	$\frac{3V_{DD}}{2}$	$\frac{V_{DD}}{2}$	V_{DD}	$\approx 5\%$	DNU	Dynamic prech. 0
$-V_{DD}$	V_{DD}	ϕ	$3\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2}$	V_{DD}	$\approx 5\%$	DPU	Dynamic prech. 1

by the ULV logic the optimum energy-delay curve is moved to the left in Figure 3, which yields a significant reduction in delay for low supply voltages or a specific energy level. The improvement of the current boost can be exploited in different ways. Firstly, we can for a specific ultra-low supply voltage obtain significant speed improvement. For example, assuming a supply voltage equal to 330mV the delay can be reduced to approximately 5% compared to standard CMOS at the same energy level. Secondly, if a system is required to operate at a certain speed, we can for meet the speed requirement for a lower supply voltage for the ULV logic than for standard CMOS. Assuming a gate delay equal to 40ps, the required supply voltage for standard CMOS is 500mV whereas the required supply voltage for the ULV logic is 250mV. The energy consumed by the ULV logic will be approximately 25% compared to standard CMOS. Hence, the ULV transistors can be exploited for ultra low-voltage and high-speed design and ultra low-voltage low-energy design.

III. ULV AND AND NAND GATES

Different applications of the ULV domino inverter is shown Figure 4. The inverters can be used to implement AND2 and NAND2 functions by using one of the inputs to set the precharge level. The gates in Figure 4 can be described as a pass transistor with an increased current level. The delay of the gates are dependent on the input delay. If we consider the gate in a) we observe that the evaluate transistor E_n acts as a pass transistor for the input \bar{B} when \bar{B} switches from 1 to 0 and the other input A switches from 0 to 1. The delay of the AND2 and NAND2 gates are less than 8% of a standard complementary NAND gate for supply voltages below 500mV. For a supply voltage equal to 300mV the delay of a NAND2 gate is 310ps whereas the delay for a complementary NAND2 gate is more than 6ns.

The different configurations of the AND/NAND ULV gates are given in Table II. Consider the NAND gate in Figure 5 a). The response of the gate is depending on the clock signals and inputs:

- Figure 5 b) $\phi = 1$, precharge. The output is precharged to 1 and the gate of the evaluate transistor E_n and E_p are recharged to 0 and 1 respectively. The input A is precharged to 0 and the input \bar{B} is precharged to 1.
- Figure 5 c) $\phi = 1$ and $A = 0$ (no change) and $\bar{B} = 1$ (no change). The gate of the evaluate transistors are not changed and the output remains high.

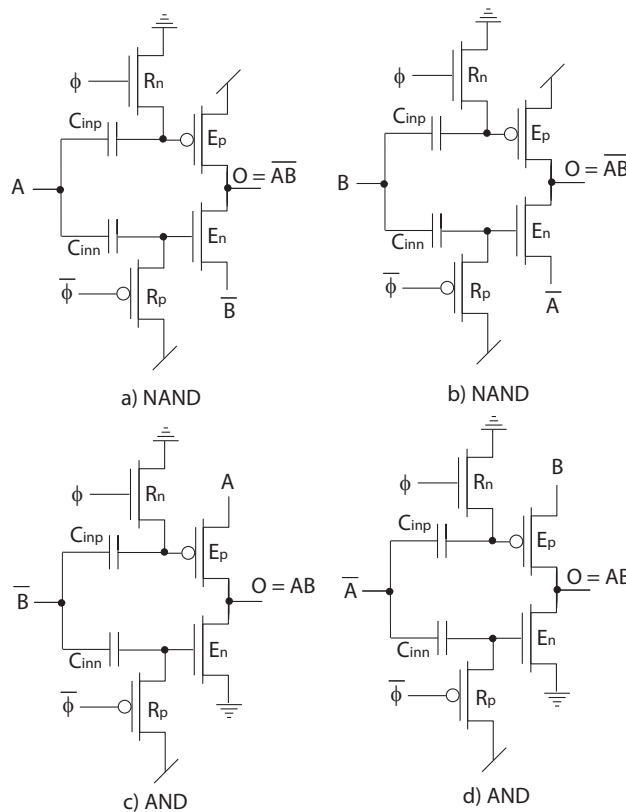


Figure 4: ULV domino AND and NAND gates.

- Figure 5 d) $\phi = 1$ and $A = 0$ (no change) and $\bar{B} = 0$ (transition). The output remains high due to a strong pMOS evaluate transistor E_p .
- Figure 5 e) $\phi = 1$ and $A = 1$ (transition) and $\bar{B} = 1$ (no change). The nMOS evaluate transistor E_n is enhanced and the pMOS evaluation transistor E_p is weakened. The output will not be affected by this condition.
- Figure 5 f) $\phi = 1$ and $A = 1$ (transition) and $\bar{B} = 0$ (transition). The nMOS evaluate transistor E_n is enhanced and the pMOS evaluation transistor E_p is weakened and the output will be pulled to GND (0) by an enhanced nMOS evaluate transistor.

An alternative and simplified NAND gates using an ULV pass transistor is shown in Figure 6 a). The NAND gate in recharge/precharge mode, i.e., output precharged to 1 and inputs B and \bar{A} precharged to 0 and 1, is shown in b) and the simplified circuit equivalents for different inputs are shown

Table II: DIFFERENT CONFIGURATIONS

A	B	O	Function
A	\bar{B}	O	a)
0	0↓	1	NAND
0	1	1	NAND
1↑	0↓	0↓	NAND
1↑	1	1	NAND
\bar{A}	B	O	b)
0↓	0	1	NAND
0↓	1↑	0↓	NAND
1	0	1	NAND
1	1↑	1	NAND
A	\bar{B}	O	c)
0	0↓	0	AND
0	1	0	AND
1↑	0↓	1↑	AND
1↑	1	0	AND
\bar{A}	B	O	d)
0↓	0	0	AND
0↓	1↑	1↑	AND
1	0	0	AND
1	1↑	0	AND

in Figure 6 c) to f). For input $\bar{A} = 1$ (no change) shown in c) and d) the output will remain high. Details of operation are:

- Figure 6 c) $B = 0$ (no change) and $\bar{A} = 1$ (no change). The output remains high unless some other circuitry pull the output down to 0 by an enhanced nMOS transistor. If so the gate of the evaluate transistor will be pulled to 0 and turn off the evaluate transistor E in order to prevent the output to affect the input \bar{A} .
- Figure 6 d) $B = 1$ (transition) and $\bar{A} = 1$ (no change). The evaluate transistor E is enhanced and the output will remain high unless some other circuitry pull the output down to 0 by an enhanced nMOS transistor. If so the gate of the enhanced evaluate transistor will be pulled to 0 and turn off the evaluate transistor E in order to prevent the output to affect the input \bar{A} .
- Figure 6 e) $B = 0$ (no change) and $\bar{A} = 0$ (transition). The evaluate transistor E is not enhanced and the output may be pulled to 0 or remain high depending on other circuitry. If there are no other transistor driving the output, the output will be pulled slowly towards 0. The time constant for the pull-down is however much higher than the time constant for an active pull-down by an enhanced evaluate transistor.
- Figure 6 f) $B = 1$ (transition) and $\bar{A} = 0$ (transition). The output is pulled to 0 by the enhanced evaluate transistor E .

IV. ULV CARRY GATES

We can use the NAND gates shown in Figure 4 to implement a high speed ULV carry function. By combin-

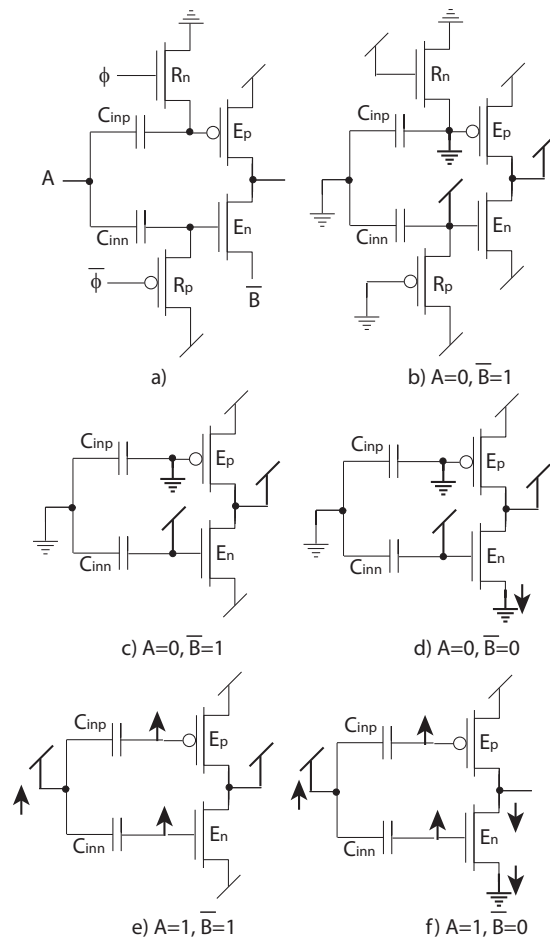


Figure 5: Simplified circuit equivalents for the NAND gate.

Table III: TRUTH TABLE FOR CARRY GATE

C_{in}	A	B	\bar{A}	\bar{B}	\bar{C}_{out}	C_{out}
0	0	0	1	1	1	0
0	0	1↑	1	0↓	1	0
0	1↑	0	0↓	1	1	0
0	1↑	1↑	0↓	0↓	0↓	1↑
1↑	0	0	1	1	1	0
1↑	0	1↑	1	0↓	0↓	1↑
1↑	1↑	0	0↓	1	0↓	1↑
1↑	1↑	1↑	0↓	0↓	0↓	1↑

ing three NAND2 gates we obtain the carry defined by $\bar{C}_{out} = \bar{A}B + A\bar{B} + \bar{C}_{in}$. Furthermore, we may assume that the inputs A and B will arrive prior to the carry input signal in a serial carry propagation chain. By applying the A and B inputs to the source of the evaluate transistors we minimize the worst case propagation delay. If $A \neq B$ the carry output is only dependent on the carry input, which is the worst case scenario for a serial adder.

A ULV carry gate is shown in Figure 7. By using 3 ULV NAND gates from Figure 4 we can implement the

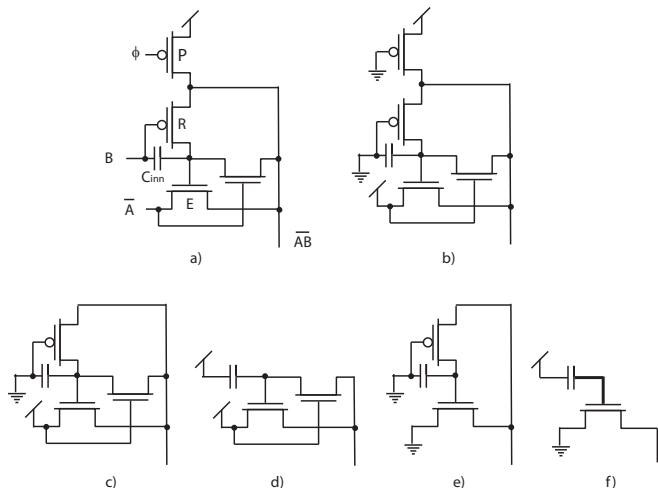


Figure 6: NAND ULV pass transistor gates.

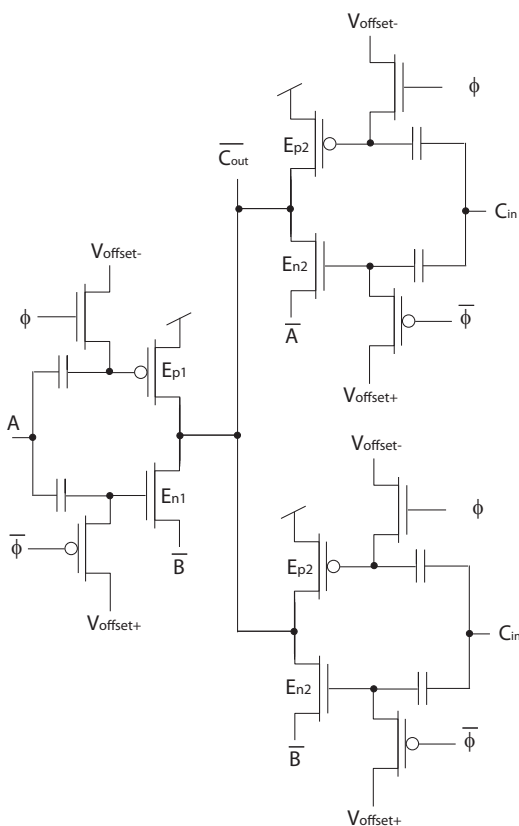


Figure 7: $\overline{C_{out}} = \overline{AB + AC_{in} + BC_{in}}$.

carry invert function. The carry input C_{in} is applied to the evaluate transistors of two NAND gates. The output carry is precharged to logic one whereas the input carry is recharged to 0. Alternate carry bits have different polarities, as shown in Figure 8. The truth table is shown in Table III.

Preliminary simulation data for the ULV carry chain using the carry gates in Figures 7 and 8 is shown in Figure 9. The

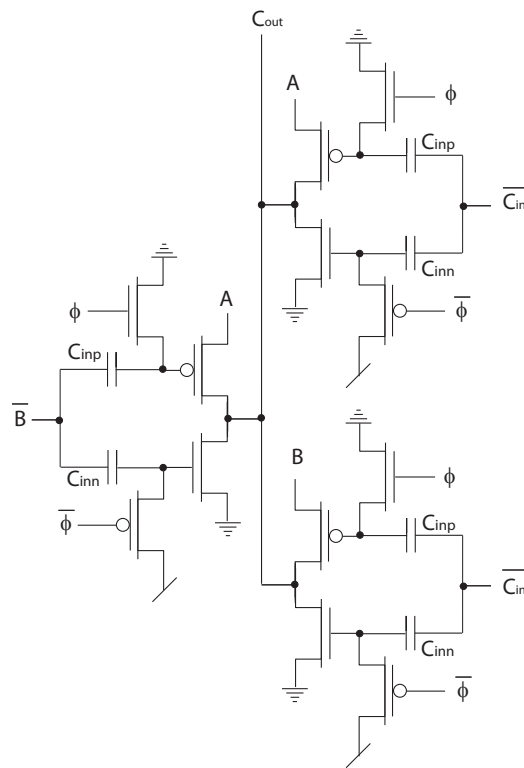


Figure 8: $C_{out} = AB + AC_{in} + BC_{in}$.

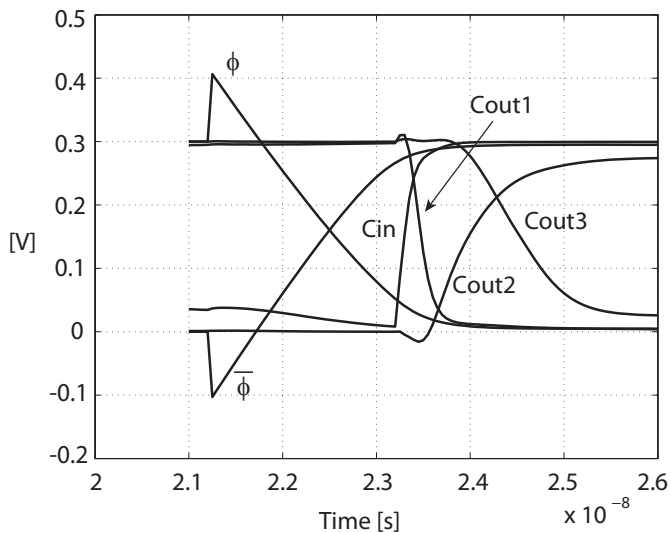


Figure 9: Preliminary simulation data for the ULV carry chain.

clock signal ϕ and $\bar{\phi}$ are provided by large complementary inverters and the large fall and rise time compared to the ULV carry gate of these signals are evident. The delay through a complementary inverter is $2.2ns$ and the delay for a complementary carry gate is more than $5ns$ for a supply voltage equal to $300mv$. The delay for the ULV carry chain is $175ps$ for bit 1, $501ps$ for bit 2 and approximately $650ps$

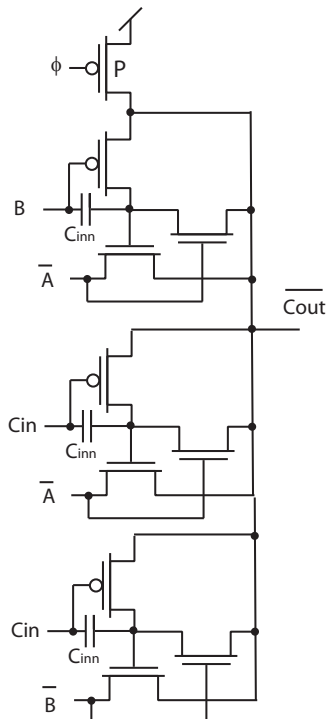


Figure 10: Alternative carry gate using pass transistor.

for the following bits.

An alternative carry gate exploiting the NAND gates in Figure 6 is shown in Figure 10. This gate has less transistors and less capacitive input load than the carry gate in Figure 7. The carry input signal is used to initiate the precharge the output, hence the output will be precharged to 1 until the input carry signal arrives unless the carry output is pulled to 0 by $A = B = 1$. Note that the carry signals is only applied to recharge transistors and input capacitors and not as pass inputs. The carry input is precharged to 0, which turns on the recharge transistors. In the same phase, the output is precharged to 1 while the inputs \bar{A} and \bar{B} are precharged to 1.

V. CONCLUSION

The potential of ultra low-voltage domino and pass transistor CMOS has been presented. Different NAND and AND gates have been presented and are applied in ULV carry chains. Preliminary simulation results shows potential speed improvement of the proposed carry gates compared to complementary CMOS by a factor of 10 or more. Simulated data are based on *SpectreS* simulator provided by *Cadence* and are valid for 90nm TSMC CMOS process.

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Robustness of the Ultra Low-Voltage Domino Gates CMOS

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Abstract—In this paper, we elaborate on the dimensioning of the ultra low voltage gate with keeper. We compare the gate configuration to ULV5 and demonstrate the potential and weaknesses of the new gate configuration with the keeper. We also pinpoint the crucial signal paths (mainly regarding the clock drivers) while also providing an overview of the propagation through a chain of gates.

Keywords—NP domino logic; ultra low voltage; floating-gate; CMOS, high-speed; clock drivers; 90 nm process.

I. INTRODUCTION

For decades, technology has been driven by scaling the size of the transistor. We have evolved a fabrication process to reduce the size from several micrometres (μm) to tens of nanometres (nm). The heart of technology is the transistor and it has been one of the key components that has allowed the plethora of portable electronic gadgets that enrich our everyday lives. Unfortunately, millions of transistor chips fabricated using modern processes suffer from very low yields (<50%) [1]. Meanwhile, the consumer market has dramatically increased demand for sophisticated portable electronics, such as handheld computers and smart-phones.

Portable electronics drive the need for low power and low voltage due to a limited budget set by a fixed maximum battery mass. Soon, we will see research toward embedded circuits in human bodies and the need to harvest energy will become more evident. Several approaches exist to lower the energy consumption. One of the most fundamental and effective approaches is to lower the supply voltage [2], [3], [4]. When the supply voltage is reduced to hundreds of millivolts, it is known as Ultra Low Voltage (ULV) [5], [6]. However, scaling of the supply-voltage has an adverse effect on the speed of operation of the design. The main challenge is to obtain high speed at supply-voltages that are as low as possible. To maintain good response times at ultra low supply voltages, the threshold voltages of the transistors must also be reduced [7]. Unfortunately, this requires a change to the CMOS fabrication process. The multiple- V_{dd} technique has been proposed for low voltage high performance circuit designs [8] without the need to change the fabrication process. Floating-Gates (FG) have also been proposed for ULV and Low Power (LP) logic [9]. Unfortunately, modern processes face significant gate

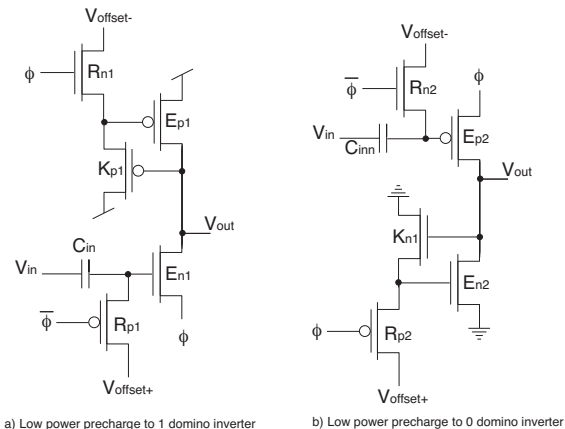


Figure 1. Low power ULV inverter based on domino logic with floating-gate. This gate configuration is known as ULV5 (the fifth modification). The symbols are recharge transistor (R_p and R_n), evaluation transistor (E_p and E_n), keeper transistor (K_p and K_n), clock signal (ϕ).

leakage due to the thin oxide. A ULV floating-gate inverter employing a frequent recharge technique has shown good properties for achieving high speed at ultra low voltages [10]. Even though the ULV gate has shown good performance it also has limitations, due the leakage at the semi-floating-gates (SFG). A differential ULV gate has been proposed which includes a keeper function [11]; it is argued to have the speed of an ULV but the stability of a standard CMOS gate.

In this paper, we elaborate more on the attributes of the ULV gate and its modification to resemble a precharge logic. Furthermore, we discuss the inclusion of a keeper transistor that enables reduction of the static power consumption. The main aim of this paper is to evaluate the advantages and reliability that the modification allows in terms of delay response, transistor matching and power consumption. We also discuss secondary effects such as clock driver dimensioning.

The structure of this paper is as follows: in Section II, the ULV5 and the keeper transistor modification of the ULV structure are presented. In Section III, a discussion of the results achieved is given. Finally, the paper concludes by

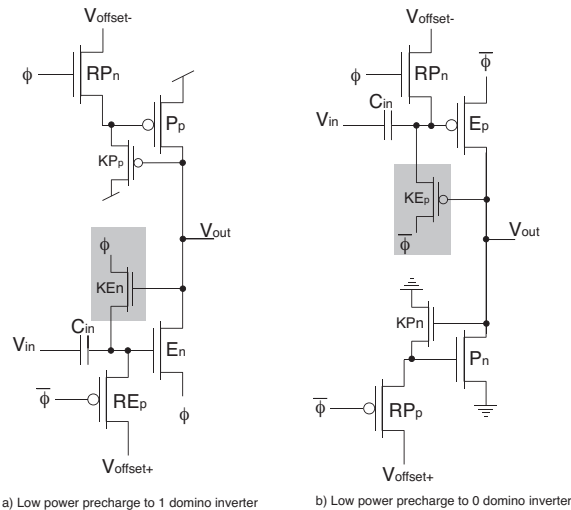


Figure 2. The ULV5 gate is modified by adding a keeper transistor (KE_n and KE_p) to the evaluation transistors, highlighted in the gray box.

highlighting the optimal design parameters. The simulation results demonstrated throughout this paper were obtained using a simulation produced in a TSMC 90 nm process environment provided by Cadence.

II. ULTRA LOW VOLTAGE GATE WITH KEEPER

The ULV gates have been presented in five evolution steps, from ULV1 to ULV5 [12], [13]. The most recent modification of ULV5 is presented in [12], with an additional improvement made by adding a keeper transistor to the evaluation transistor in the N- and P-domino logic gates. The ULV5 without the keeper transistor is illustrated in Figure 1, while modification of the gate with the keeper transistor is illustrated in Figure 2. The keeper transistors (KE_n and KE_p) are highlighted in gray. Considering Figure 2(a), the transistor KE_n would contribute to weaken the pull-down transistor (E_n) when the output (V_{out}) is to be kept high (V_{dd}). The signal flow for a precharge 1 domino inverter with the keeper transistors would be as follows, for input with:

- (a) **Non-transition** - The output is to be kept high. The KE_n would be turned off, the gate of P_p would be low (0) and hence V_{out} is held high through P_p to V_{dd} . The feedback from the keeper transistor KE_n would pull the floating-gate at the input of E_n to the source of the KE_n , which, at the time, would be 0 ($\phi = 0$). Given time, the keeper transistor KE_n would turn the E_n completely off and moreover significantly lower the static power consumption during the evaluation period.
- (b) **Positive transition** - The output would, as a result of the input transition, be pulled towards 0 through the E_n -transistor. As the output V_{out} decreases, the feedback keeper KP_p -transistor would increasingly turn on and contribute to the shut-down of the pull-up transistor P_p .

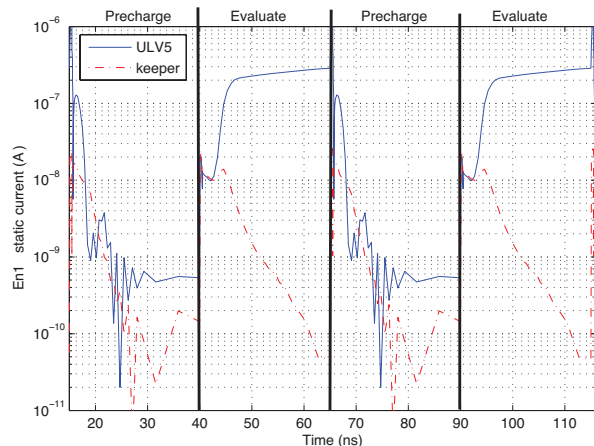


Figure 3. Simulation of a ULV5 with keeper. The plot shows the current dissipation through the E_n for the input signal with no transition (presented in section II(a)).

In turn, this would increase the speed of pulling V_{out} to 0. The more V_{out} is lowered, the weaker the keeper transistor KE_n contribution to the floating-gate at the E_n .

The main improvement made by adding the keeper transistor is the significant decrease of static power consumption. This is primarily due to the shut-down of the evaluation transistor, which competes with the precharge transistor during the evaluation period for a non-transition input. The current consumption during a clock cycle for a non-transition input for both the ULV5 and the ULV5 with keeper configurations is shown in Figure 3. The simulation results show that the keeper configuration has a current dissipation factor approximately 10,000 times lower through the E_n .

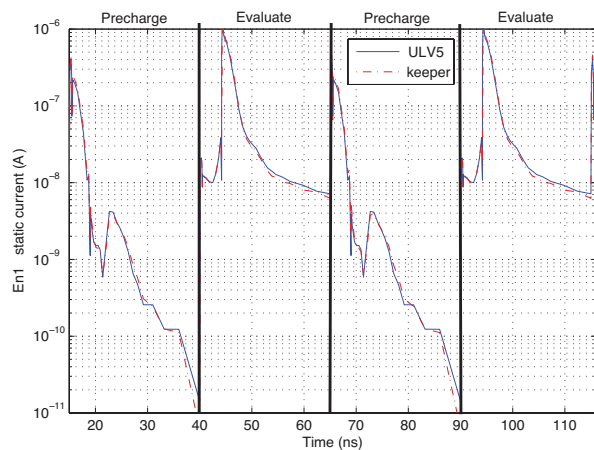


Figure 4. The simulation of a ULV5 with keeper. The plot shows the current dissipation through the E_n for the input signal with a positive transition (Section II(b)).

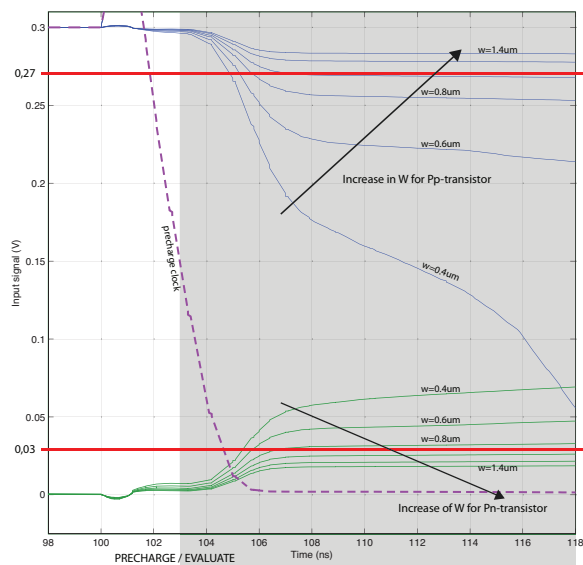


Figure 5. Parametric simulation with changes based on the width of the precharge transistors. The plot shows the evaluation period for a ULV5 (without keeper), and its ability to hold the output (V_{out}) for the case of a non-transition at the input (Section II(a)).

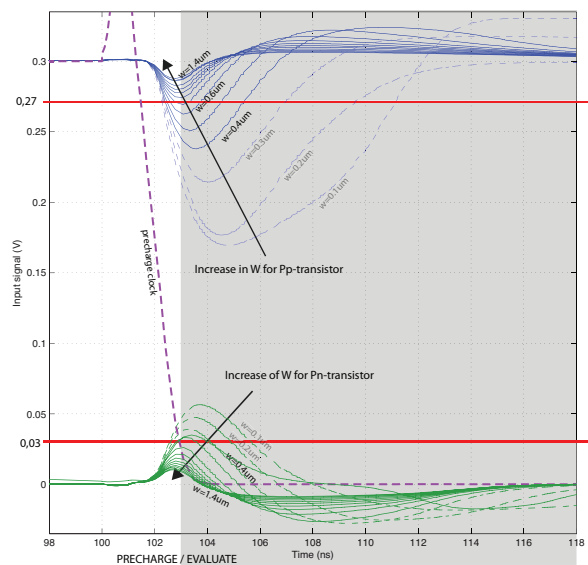


Figure 6. Parametric simulation for the ULV5 with keeper. The width of the precharge transistors are parameterised for the case of a non-transition at the input during an evaluation period. This plot is based on the same simulation environment as for the ULV5 without the keeper, shown in Figure 5.

During the precharge period, the current dissipations are different due to the starting point of the floating-gates and the specific DC voltage at the output V_{out} . For a positive input transition the current dissipation is equal, hence the high speed of the gate is ensured. The simulation result for the gate with a positive transition is shown in Figure 4. The ULV5 with keeper configuration is therefore a great improvement in terms of static power, while all other beneficial attributes are maintained compared with standard CMOS. In the following section, we are to elaborate on the details of the different elements within the gate. We aim to analyse which dimension gives the best overall effect.

Table I
THE TRADE-OFF FOR DELAY AND LOAD FOR THE ULV5 WITH KEEPER.

(μm) C_i	Time (ns)		(ns) Delay
	In 50%	Out 50%	
0.5	-	-	-
1.0	5.81	7.30	1.49
1.5	5.58	5.96	0.38
2.0	5.47	5.73	0.26
2.5	5.41	5.62	0.21
3.0	5.38	5.56	0.18
3.5	5.35	5.51	0.16
4.0	5.33	5.48	0.15
4.5	5.32	5.46	0.14
5.0	5.31	5.44	0.13
5.5	5.30	5.43	0.13

III. SIMULATION RESULTS AND DISCUSSION

We start by elaborating on the effect of the capacitive input to the gates. The dimension of the input capacitance (C_i) directly affects the gate by attenuating the transition (the input voltage swing) and thus increasing the delay. The lower C_i is, the more significant the role the parasitic gate-capacitances play. The higher C_i is, the higher the load (C_L) that is required to burden the previous gate. Therefore, there should be a trade-off between the amount of parasitic capacitance and the load. Our parametric simulation for the gate with keeper configuration considering parameterisation of C_i is shown in Table II, with focus on the gate delay. From the table, we have chosen to use a 2.5 fF input capacitance. The input capacitance for the N- and P-domino gates has different input gates, hence nMOS and pMOS; therefore considerations must be made regarding matching of the nMOS and pMOS transistors for both evaluation and precharge. Transistor matching for the nMOS and pMOS for these low supply voltages (V_{dd}) has different mobility abilities. Matching of the nMOS and pMOS for a standard CMOS inverter is shown in Table II. The dimensions of the evaluation transistors are preferably kept at a minimum, especially concerning matching of the C_i . This leads to the dimensioning of the precharge transistors, hence these directly affect the matching of the evaluation-transistors and the precharge through relative values. The other side-effect of changing the precharge transistors is the fact that the

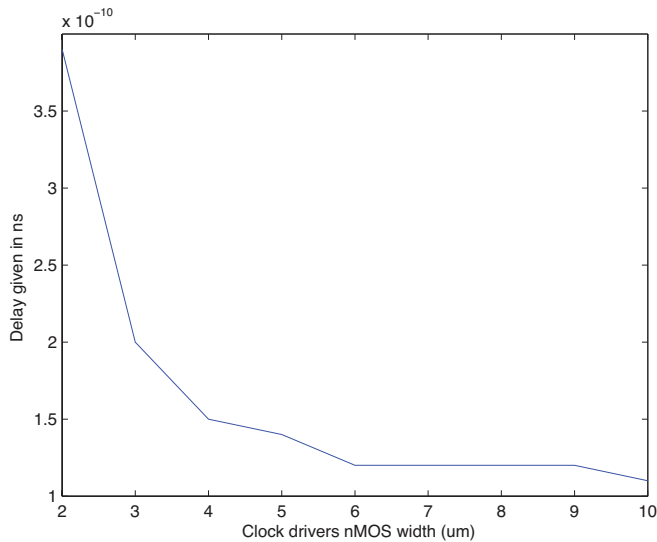


Figure 7. Simulation plot regarding the delay of the clock drivers dependency on the width of the nMOS of the clock driver.

precharge delay would be either longer or shorter. The delay in precharge (isolated) is of no concern due to the fact that we can use a skew clocking strategy, and the only aspect of importance is the DC value of the level, either V_{dd} or ground. The other consideration when dimensioning the precharge-transistors is their ability to hold the signal. This is of particular importance for the ULV5 configuration. As shown in Figure 5, the larger the width of the precharge transistor the better, and the longer it holds the output value in the case of a non-transition. For the ULV5 with the keeper configuration, shown in Figure 6, we see that holding of the value is of no concern. We would particularly like to stress the fact that a ULV5 with keeper can actually have a configuration with width of the precharge transistor as small as 100 nm. In this case, we are able to lower the area consumption for an overall perspective. One potential issue which needs to be addressed is that, contrary to

Width (μm)	
pMOS	nMOS
0.50	0.57
1.00	1.15
2.00	2.95
3.00	4.85
4.00	6.80
5.00	8.80
6.00	11.00

Table II

MATCHING OF THE NMOS AND PMOS FOR A STANDARD CMOS INVERTER GATE, SIMULATED WITHIN THE SAME CONDITIONS AS THE REST OF THE GATES IN THIS PAPER. THE SUPPLY VOLTAGE IS SET TO 300 mV.

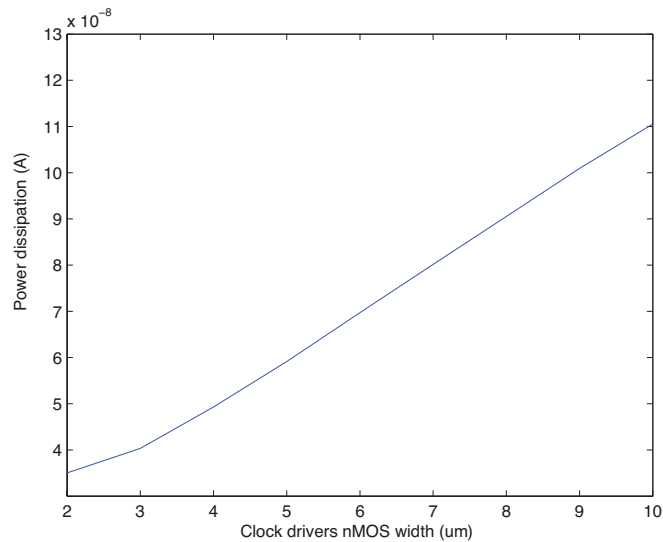
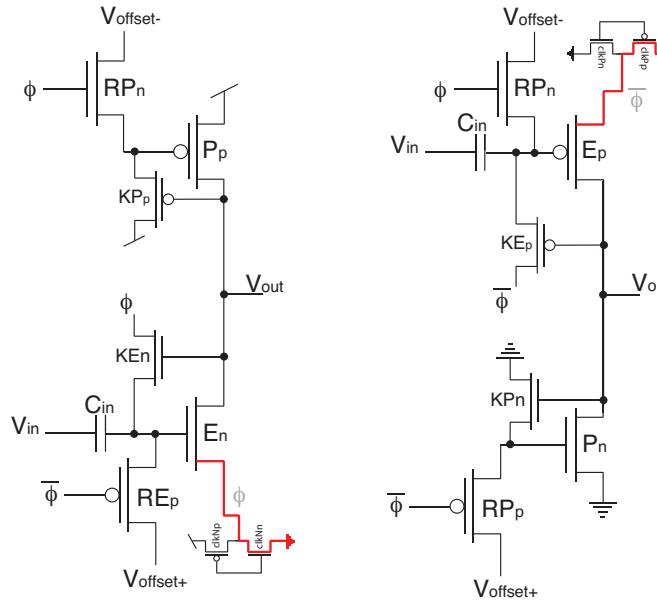


Figure 8. Simulation plot for the power dissipation through the clock driver for the specified gate based on the parameterised width of the nMOS.

CMOS domino logic, the clock signals (drivers) play a more dominant role. The clock signals are not only connected to the gate node of the transistors, but also to the drain/source of the evaluation transistors, specifically to the E_n , E_p , KE_n and KE_p transistors. Hence the clock drivers must be strong enough to not become a bottleneck for the evaluation. The most crucial path is for the E_n and E_p . In Figure 9, the critical path is shown in red. In the case shown in Figure 9(a), of an evaluation for a positive transition at the input, the evaluation transistor E_n must pull the output V_{out} down to ground. The critical path shows that the nMOS of the clock driver has a bottleneck issue; it must be large enough to pull through all the current dissipation and at the same time not increase the overall power dissipation. Our simulation results indicate that the optimal size for the nMOS width of the clock-driver is $4.0\mu\text{m}$, with a length of 200 nm. The pMOS is kept minimum, thus the pull-up and pull-down of the clock driver is skew matched. Figure 7 shows the effect of the delay of the gate with regard to the increase in the width, while in Figure 8 illustrates the power consumption through the same node. Figure 10 and Figure 11 show the energy (PDP) and the EDP, respectively.

IV. CONCLUSION

In this paper, we have elaborated on the matching and dimensioning of different elements of the ULV gate. We have demonstrated the potential improvement concerning static power dissipation of the ULV5 with keeper configuration compared with the unmodified ULV5. Furthermore, we have discussed the importance of the clock drivers dimensions. In particular, we have considered the issue of bottlenecks for



a) Low power precharge to 1 domino inverter b) Low power precharge to 0 domino inverter

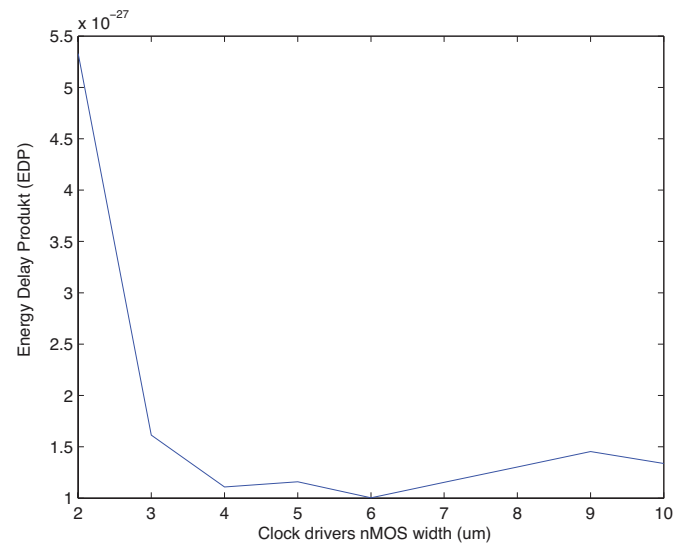


Figure 11. Calculated values for the EDP for different widths of the clock drivers nMOS.

Figure 9. The ULV5 with keeper domino gate, with single clock driver. The highlighted critical path is shown in red.

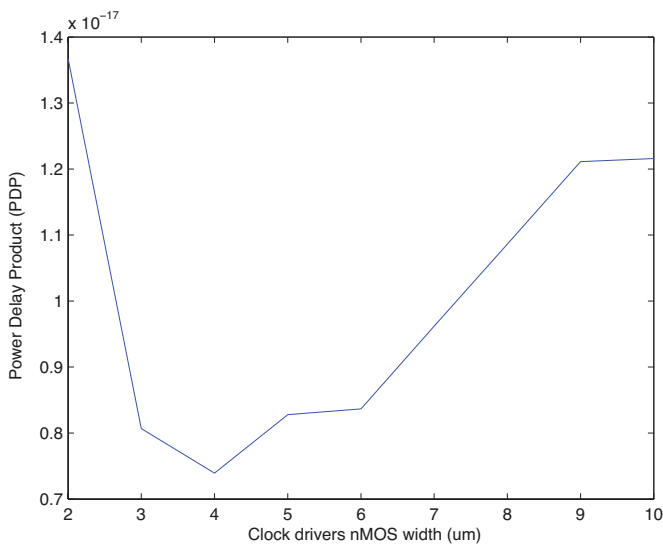


Figure 10. Simulation plot for the calculated energy (PDP) dissipation for the clock driver based on the parameterised width of the nMOS.

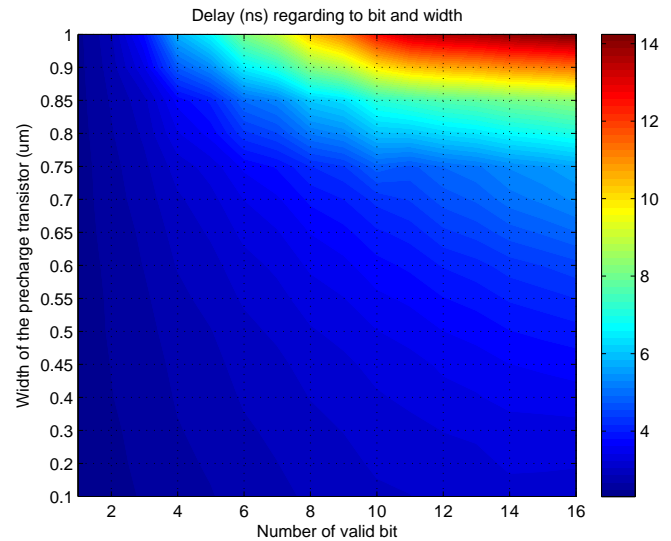


Figure 12. The ULV5 without the keeper is simulated to plot the relation between number of bits in a chain and the width of the precharge transistor. The delay is given in ns. The evaluation transistor size is kept minimal.

the evaluation transistors. The optimal values obtained in this work are $C_i=2.5$ fF, and the width of the clock driver (crucial path) is $4.0\mu\text{m}$, with a length of 200 nm. The supply voltage was 300 mV and all transistors were kept to a minimum size except for the precharge transistor. The optimal dimensions for the precharge depend on the delay and the length of the chain used for each design. For the ULV5 without the keeper, we have simulated the relationship between the number of

bits in a chain and the width of the precharge transistor. The delay is plotted in Figure 12, and the representative hold time (the time-slot which holds the output value valid) is shown in Figure 13. Finally, Figure 14 shows the valid bits and the same configurations. There was a significant improvement for the ULV5 with keeper, especially in holding a value valid, resulting in a higher bit chain.

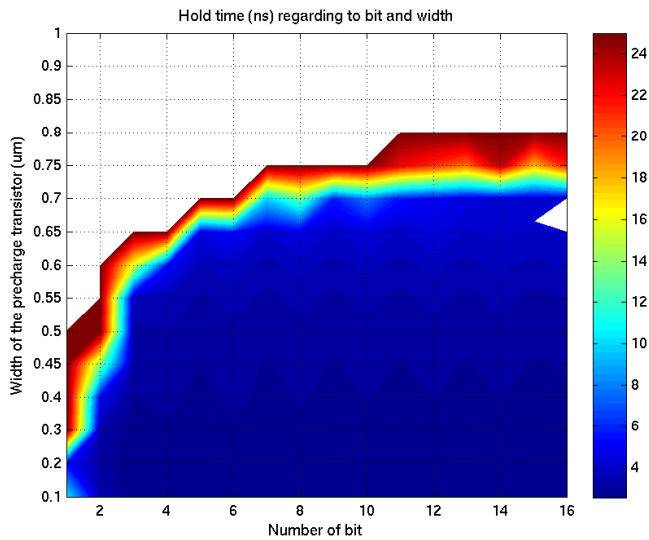


Figure 13. The ULV5 without the keeper is simulated to plot the relation between number of bits in a chain and the width of the precharge transistor. The hold time (the time-slot over which the output is kept valid) is given in ns.

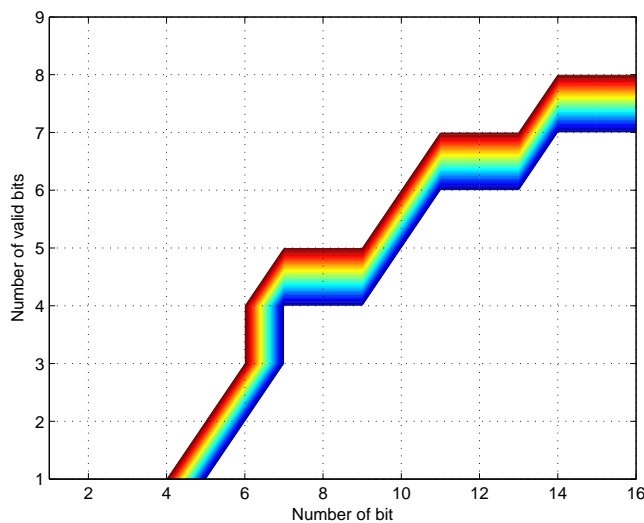


Figure 14. The simulation plot shows the development of the valid bit through the chain for different widths of the precharge transistor.

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High-frequency One-port Colpitts SAW Oscillator for Chemical Sensing

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Abstract—This paper reports upon the design and development of a low cost, high sensitivity, high frequency surface acoustic wave resonator (SAWR) based system for gas sensing applications. The 262 MHz one-port SAWR operates in a grounded-base Colpitts oscillator arrangement that was developed based on an equivalent circuit model. Electrical characteristics of the fabricated SAWR show good agreement with its equivalent device model at the resonant frequencies, and it was found to have good stability and sensitivity with a Q-factor in air of about 2,870 at its fundamental resonant frequency. The sensor system is designed to operate in a dual configuration in which one resonator is coated with a gas-sensitive polymer (polyethylene) coating, whilst the second one is used as a reference channel; thereby eliminating common mode interferences on the baseline signal. Mass sensitivity was found to be ca. 1 Hz/ng, which corresponds to sub-ppm sensitivity to gas/odour concentration.

Keywords—acoustic waves; one-port; Colpitts oscillator; BVD model; SAW resonator; polymer coating

I. INTRODUCTION

Both bulk acoustic and surface acoustic wave (SAW) based sensor systems have been reported in chemical sensing applications over the past few decades [1–4]. Due to their high sensitivity and simple drive/readout circuitry, more recent focus has been on surface acoustic wave based devices where a SAW device forms the frequency selective component within an oscillator circuit. Polymer-coated SAW based chemical sensors impart high sensitivity and selectivity to specific volatile compounds. The absorption of the ligand molecule onto the polymer changes the physicochemical and electrical behavior of the SAW device resulting in a change in its oscillation frequency.

Common methods to implement SAW oscillator circuits are typically based on the feedback loop method or the negative resistance method [5], [6]. The frequency stability and vapor sensitivity of the SAW sensor system directly depends on the type of the employed oscillator circuit. Nimal *et al.* [7] have recently reported that one-port Colpitts oscillators are more sensitive, but less stable, than two-port Pierce oscillators. The sensitivity can also be improved by tuning the phase point set within the SAWR in the pass band thereby reducing the noise performance of the oscillator circuit [8].

In this study, we present one-port polymer-coated Rayleigh wave based SAW resonators, fabricated on an ST-

cut quartz wafer, for application in low-cost chemical sensors. An investigation into different equivalent circuit models is also presented, which lead to the conclusion that the most suitable oscillator circuit for one-port SAWR sensors is a Colpitts oscillator configuration.

II. ONE PORT SAW RESONATOR

SAW resonators are commonly available as one-port and two-port devices employing either delay line or resonator configurations. Because of the potential for high Q-value, low noise level and higher stability, we have selected a one-port resonator structure. These resonators are designed to operate at a baseline frequency of 262 MHz in a dual configuration to obtain differential measurements (Fig. 1).

The design and modeling of surface acoustic devices are normally carried out using the well-established Coupling of Modes (COM) theory [9], [10]. Although a COM model allows for an accurate description of the SAW resonator by simulating the admittance behaviour, the formulas are somewhat cumbersome and are not very informative - as far as circuit analysis and simulation is concerned. In addition, the accuracy of this model is limited to a narrow frequency band around the resonance region. Hence, the COM theory must assume *near-resonance* frequencies in order to derive a simplified electrical model of the SAW resonator [11].

The Butterworth Van Dyke (BVD) model, as a simple electrical equivalent circuit model, is more suitable for circuit designers. Morgan [12] established that the electrical acoustic impedance behavior of a SAW device, obtained using a lumped-element equivalent circuit model, is in good agreement with conventional COM analysis. This equivalent circuit model conveniently relates the acoustic perturbations due to surface mass loading in a SAW device to its electrical behavior.

A BVD model [11] was developed for the 262 MHz one-port SAWR, shown in Fig. 2., allowing quick simulation and design of the associated oscillator circuitry. The motional and static arm parameters were extracted using the transmission parameters of the SAWR. As shown in Fig. 2, the electrical components R, L and C are the motional inductance, capacitance and resistance respectively, which form the *motional arm* producing the resonant frequency while the capacitor C_0 forms the *static arm* providing the anti-resonant frequency. The motional arm signifies the electro-acoustic properties [13] of the piezoelectric material and it models the vibration of the crystal. R represents the

acoustic attenuation in the resonator and capacitance C_o the capacitance of the piezoelectric crystal.

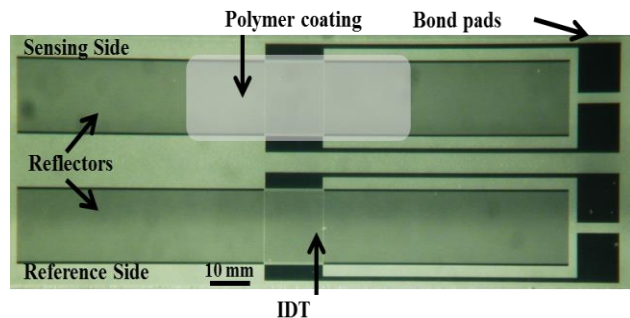


Fig.1. Optical micrograph of the 262 MHz one-port dual SAW resonator sensor, fabricated in aluminium on a ST-cut quartz wafer substrate. The top resonator is coated with a chemically-sensitive non-conductive polymer (polyethylene) and the bottom resonator is uncoated thus acting as a reference channel.

The designed 1-port SAWR comprises 60.25 finger pairs with 3 μm finger width forming the inter-digitated-transducer (IDT), and 500 reflectors on each side to create a standing wave pattern with an overall die size of 7.4 mm \times 2.4 mm. The dual resonator configuration [14] with a reference channel eliminates common mode interferences on the baseline signal, such as changes in ambient temperature or pressure. The SAWRs were fabricated on an ST-cut quartz substrate with aluminum IDTs using UV lithography (PacTech, Germany).

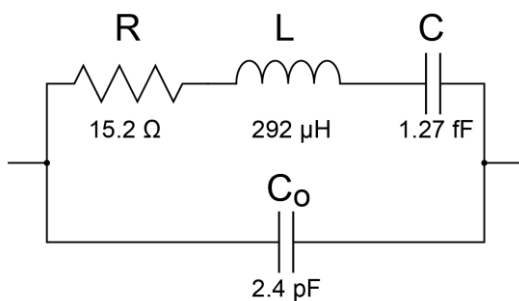


Fig.2. Illustration of the BVD equivalent circuit lumped element model of a one-port SAW resonator.

In addition to the fundamental mode of operation, the SAWR exhibits several overtone frequencies, which can be modelled by adding additional series-resonant branches to the BVD model. For operation around a certain resonant frequency, the crystal can be modelled by the circuit with a single motional arm. The impedance of this modelled circuit is given by [15]:

$$Z(s) = \frac{s^2 + \left(\frac{R}{L}\right)s + \omega_s^2}{sC_o \left[s^2 + \left(\frac{R}{L}\right)s + \left(1 + \frac{C}{C_o}\right)\omega_s^2 \right]} \quad (1)$$

where

$$\omega_s = 2\pi f_s = \frac{1}{\sqrt{LC}} \quad (2)$$

$$f_s = \frac{1}{2\pi\sqrt{LC}} \quad (3)$$

Here, f_s is the series resonance frequency of the SAWR, modeled by the motional arm. The unloaded quality factor of a SAWR is given by

$$Q_u = \frac{\omega_s L}{R} \quad (4)$$

Due to the high Q-factor of a SAWR, R can be neglected. Thus (1) becomes,

$$Z(s) = \frac{s^2 + \omega_s^2}{sC_o \left[s^2 + \left(1 + \frac{C}{C_o}\right)\omega_s^2 \right]} \quad (5)$$

This shows that the resonator exhibits a parallel resonance at:

$$f_a = \frac{1}{2\pi\sqrt{LC_T}} \quad (6)$$

where

$$C_T = \frac{CC_o}{C+C_o} \quad (7)$$

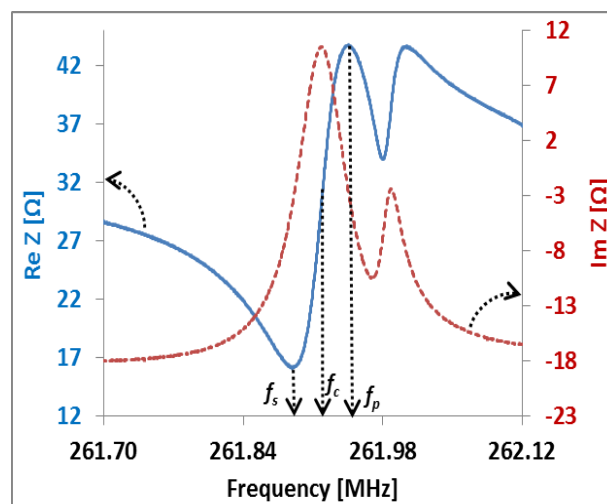


Fig.3. Real (Solid line) and imaginary parts (dotted line) of the impedance presented by 262 MHz one-port SAWR. The series, parallel and center frequencies are marked on the diagram.

The real and imaginary parts of the one-port SAWR impedance exhibiting a minimum resistance at resonance and a maximum resistance at anti-resonance frequencies, obtained by an RF network analyzer (E5071B, Agilent Technologies), is shown in Fig. 3. The series resonance frequency, f_s , is 261.91 MHz, the parallel resonance, f_a is 261.94 MHz and the center frequency, f_c is 261.92 MHz. This also demonstrates that the SAWR center frequency lies

as expected between the series and parallel resonant frequencies. The phase curve in Fig. 3 also shows that the Barkhausen criterion of 0° phase condition for oscillation is satisfied at the center frequency of the SAWR.

III. COLPITTS OSCILLATOR DESIGN

Several similar transistor-based circuit configurations are available for the realisation of SAW oscillators, such as Pierce, Colpitts, and Clapp, with the main difference lying in the transistor grounding options. The performance of the three configurations varies with the difference in the position of the biasing resistors and capacitances. The most desirable option is the Pierce configuration due to its simplicity, robustness and ability to work at higher frequencies (> 500 MHz) because it is arguably the least affected by stray capacitances [15]. However, the Pierce oscillator can only work with a two-port SAW resonator within a feedback loop to attain the required 180° phase shift.

The Colpitts oscillator, however, allows the SAWR to operate in a 1-port configuration [7], and therefore was selected for this work. The schematic of the Colpitts SAW oscillator circuit with a grounded base configuration, where the SAWR input is connected to the transistor's base and the output port is connected to the ground, is shown in Fig. 4.

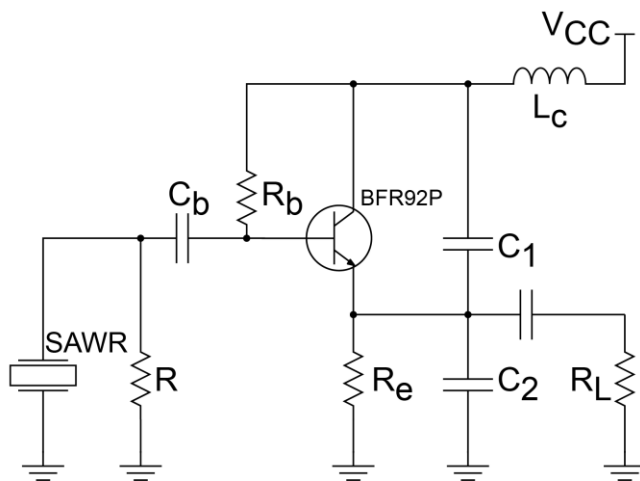


Fig. 4. Simplified schematic of the Colpitts oscillator circuitry used to drive the 1-port SAW resonator sensor.

The Colpitts oscillator offers good stability at higher frequencies, lower harmonics, lower component count and hence lower cost than other types including feedback-based oscillator. The transition frequency of the transistor, f_T , limits its frequency of operation, when the capacitors needed for obtaining the oscillation frequency are comparable to the transistor's terminal capacitances. This may be avoided by using a high f_T value (a few gigahertz) BJT in the oscillator circuit or by using the crystal in a series resonance configuration [15]. The use of RF transistor (BFR92P, Infineon) rather than an operational amplifier also

reduces parasitic capacitances allowing radio frequency (RF) oscillator operation. To obtain the tuned oscillation frequency close to the SAWR Q-factor, tight tolerance components were selected for the capacitor and the inductor values.

In this configuration, the resonator shows an inductive behavior between the series (f_s) and parallel resonances (f_p). The transistor along with the feedback capacitors C_1 and C_2 provides the negative resistance to compensate for resistive losses in the resonator. The major limitation of such an oscillator circuit is that the parasitic capacitances begin to affect the effective operation of the circuit at frequencies above 500 MHz.

IV. CHEMICAL DETECTION SYSTEM SETUP

A robust, high-sensitivity chemical detection system based on polymer-coated one port SAW sensor has been designed and implemented. The SAW oscillator has been realized by interfacing the dual SAW resonators to Colpitts oscillator circuitry. A two layered Printed Circuit Board (PCB) has been designed using Altium Designer software. Figure 5 shows the photograph of the dual Colpitts SAW oscillator based chemical sensor system. The PCB ensures minimal cross-talk associated with high frequency signals. The phase shifts linked with the RF signal paths to the resonators have also been taken into account during the PCB design.

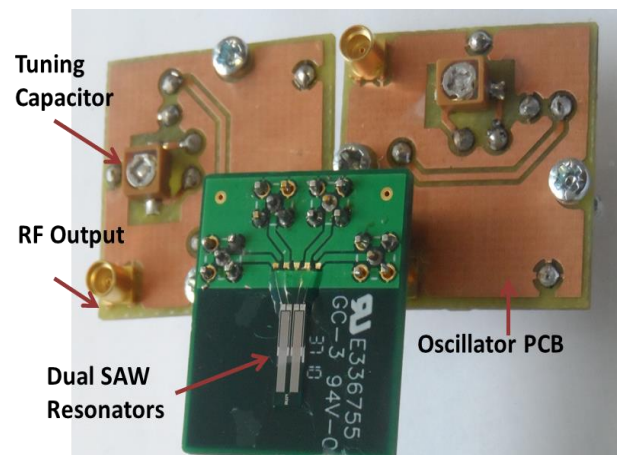


Fig.5. Photograph of the SAW resonator with associated Colpitts oscillator circuit on the backside of a custom PCB.

The experimental arrangement demonstrating chemical detection using SAW oscillator consists of a $14 \times 14 \times 40$ cm³ gas/odor chamber (photograph of the setup is shown in Fig. 6) to which a nEMESYS multi-channel syringe pump (Cetoni GmbH, Germany) is attached. The microliter precision syringe delivers the chemicals into the chamber via capillary lines, where it gets vaporised. The SAW sensors, arranged in dual configuration, where one is coated with the sensing polymer *polyethylene* and the other

sensor forms the reference channel are attached to the far end of the chamber. A commercial FQ4 interface instrument (JLM Innovation, Tubingen, Germany) was connected to the oscillator output for frequency measurement. The oscillation frequencies of the individual sensors were monitored to obtain the SAWR differential signal.

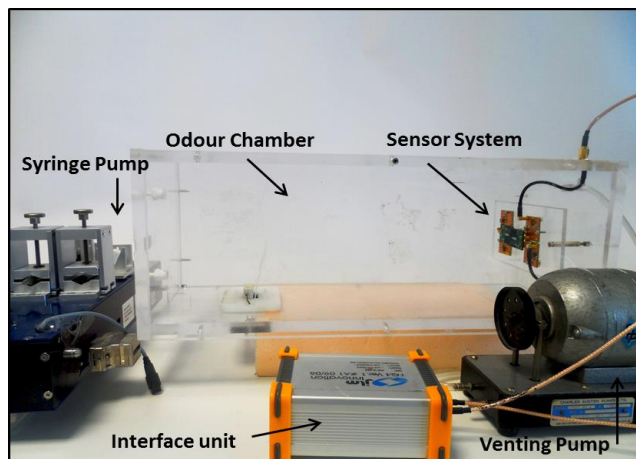


Fig.6. Experimental arrangement for chemical detection sensor system consisting of an odour chamber, a venting pump, syringe pump, and SAW sensors with the Colpitts circuitry.

V. EXPERIMENTAL RESULTS

Figure 7 shows the oscillator’s resonant frequency output obtained by an RF oscilloscope (LeCroy LT342 Waverunner). The measured frequency value is in good agreement with the theoretically modeled value. The load sensitivity is significantly less for this oscillator circuit. The output of the SAWR oscillator is practically noise and distortion free.

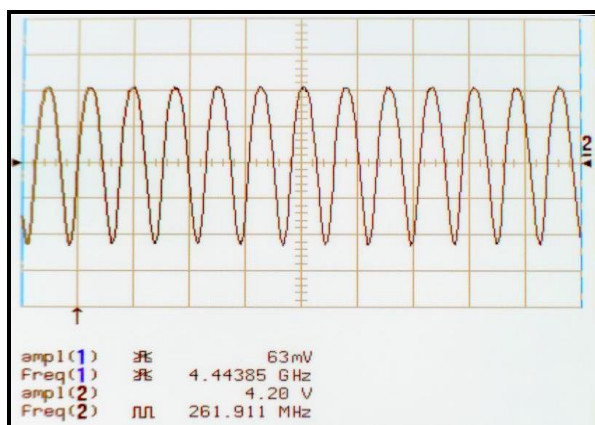


Fig.7. Photograph of the baseline frequency (261.9 MHz with amplitude of 4.2 V) of a Colpitts SAW oscillator sensor system shown at the channel 2 of an RF Oscilloscope.

The typical frequency shifts of a dual SAWR sensor after the detection of a volatile chemical compound (here an insect sex pheromone) shows that the one-port SAW

oscillator provides a highly-sensitive system for chemical detection. The response has a low level of noise as shown in Fig. 8. On the introduction of 10 µl of the insect pheromone Z9-14:OAc into the odor chamber, a differential frequency shift of about 6 kHz was measured at the SAW output, which shows that the average sensor response to the pheromone compound is about 0.6 Hz/nl of liquid, i.e., sub-ppm levels of pheromone in air.

The response time of the system is relatively slow (~100 s) and it is associated with the evaporation and diffusion of the volatile compound inside the chamber. However, the actual response time of the SAWR itself is below one second.

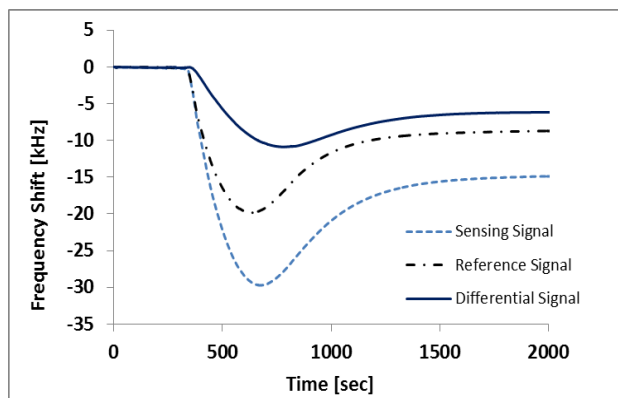


Fig.8. Differential frequency response of polymer-coated SAWR sensor to pheromone Z9-14:OAc demonstrating the high sensitivity of the polymer-coated SAWR sensor.

VI. CONCLUSION

A high frequency one-port Colpitts SAWR oscillator has been designed and fabricated for application in a low-cost, low-power gas sensor. An equivalent model has been developed, which formed the basis of an oscillator circuit design for a highly sensitive chemical sensor. The SAWR exhibits a high quality factor of 2,870 and has an estimated 0.5 Hz/ng mass sensitivity after coating with a thin gas sensitive non-conducting polymer film.

Further studies are being carried out on the detection of specific blends (i.e. mixtures) of chemical compounds. In addition, technological developments of this work include the creation of a smart low-cost, low-power chemical sensor on a chip - by the integration of the SAWR sensor with full custom CMOS oscillator circuitry thus resulting in an application-specific integrated circuit (ASIC) BioMEMS chip.

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FPGA Implementation of Disparity Estimation Processing Architecture for Stereo Camera System

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Abstract—With the advance of image processing and computer vision, the stereo vision system with two cameras has become the research of interest in many areas since its ability to realize the depth information is similar to human vision. Depth map algorithm allows camera system to estimate depth. It is a computation intensive algorithm, but can be implemented with high speed on hardware due to the parallelism property. In this paper, by analyzing digital image stabilization (DIS) algorithms, we propose an efficient disparity estimation architecture, which combines gray-scaled projection and Affine transformation model. We develop the architecture by describing the various computation units in hardware description language (Verilog) and synthesizing the design into a FPGA. The synthesis and experimental results for three video test images show that the proposed hardwired architecture is better than traditional sum of absolute difference (SAD) architecture, which based on block matching algorithm in terms of frame rate (frame/sec) while keeping the competitive PSNR results.

Keywords -Gray-scale projection; Steroscopic; architecture; 3D

I. INTRODUCTION

Recently, industrial demand and interest of stereoscopic image systems are increased due to 3D movies and HD -TV. The depth information is the main element in 3D image systems. Stereo matching or disparity estimation is exploited to find the depth information from stereoscopic images. The goals of this paper are to propose a real-time processing architecture for disparity estimation and to show application systems based on real-time stereo camera system. The proposed system operates in the FPGA board environment with stereo camera.

It has potential uses in robotic navigation, 3D imaging, camera surveillance and object recognition systems. A typical depth estimation system consists of two cameras with overlapping field of view and a processing unit. To estimate the depth, several depth-map algorithms have been developed [1]. The idea is to find the displacement between two projections of the same object in the two images. From that, the distance is calculated based on the relative position of the two cameras and other dimensions such as focal length, angle between optical axes. The depth value is represented in

the result image as pixel intensity. The depth-map algorithm is also called the disparity algorithm. The idea of a depth-map system is quite simple. However, the depth-map algorithm is computational and data intensive [2] because it has to perform an identical procedure on millions of pixel. Due to the computational complexity of the disparity algorithms, several attempts for video 3D tracking have been developed in recent years [3]. several attempts have been made[3-5], including systems implemented on personal computer, digital signal processor (DSP), field programmable gate array (FPGA) and application specific integrated circuit (ASIC). One of these attempts presented in 3D feature tracking and localization using stereo vision systems. The objective of feature localization is to localize the corresponding feature point in the right video sequence. Because the motion of the given feature point in the left and right video sequences is similar, this system is designed to obtain the motion vectors from acquired image frame of the left video sequence and to estimate the corresponding motion vectors for the feature in the right video sequence.

Various algorithms, such as projection algorithm (PA), bit-plane matching (BPM), and others, have been developed to estimate the motion vectors. In general, the gray scale projection algorithm can greatly reduce the complexity of computation in comparison with the other methods. In this paper, our focus is to develop an efficient architecture based on the motion vectors of the gray scale projection and Affine transformation model for practical implementation of 3D image processing.

This paper is organized as follows. Section II describes the algorithm of gray-scale projection and estimate motion vectors. Section III describes the design of the proposed architecture. Experimental results are shown in Section IV. Finally, the conclusion is given in section V.

II. GRAY SCALE PROJECTION

The gray-scale projection is an approach based on total gray-scale changes in the coordinate of an image to estimate Motion vectors between the current and reference frames. By doing a related operation using gray-scale projection algorithm, we can determine motion vector. A small amount of computation is one of the valuable characteristics of this algorithm. Normally, the gray-scale projection algorithm can

be divided into three steps: Image projection, projector filter, and its correlation image projection.

The gray scale projection uses gray information of image to compute the correlation between two frames. Its projection is divided into two one-dimensional wave shaped plane, these formulas are described as follows:

$$P_{vk}(i) = \sum_{j=1}^N Y(i, j) \quad (1)$$

$$P_{hk}(j) = \sum_{i=1}^M Y(i, j)$$

In which, $Y(i, j)$ is the gray value of point (i, j) at image frame k , $P_{vk}(i)$ is the vertical i projection at frame k , $P_{hk}(j)$ is the horizontal j projection at frame k , the size of frame is $M \times N$.

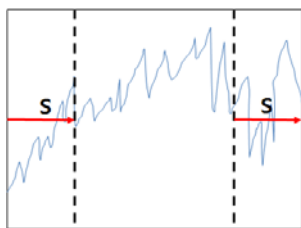


Figure 1. Results of horizontal and vertical gray projection curve at frame k .

Figure 1 shows results of the horizontal and vertical projection at frame k . S denotes the invalid width of search between the current frame and the reference frame.

A. Correlation calculation

In order to estimate the motion vectors, we can perform the correlated operations with vertical gray-scale projection curves [4] of left image frame and horizontal gray-scale projection curves of right image frame respectively. Thereby, we can obtain two cross-correlation curves. According to the local minimum value of two curves, we can get a motion vector between left image and right image [5]. The correlation computing formulas are described as follows:

$$C_v(w) = \sum_{i=1}^{M-2S+1} |P_v^l(i+w-1) - P_v^r(i+S)|, (1 \leq w \leq 2S+1) \quad (2)$$

$$C_h(w) = \sum_{j=1}^{M-2S+1} |P_h^l(i+w-1) - P_h^r(i+S)|, (1 \leq w \leq 2S+1) \quad (3)$$

In which, $P_v^l(i+w-1)$, $P_h^l(i+s)$ are the vertical and horizontal projection curves of the left frame and $P_v^r(i+w-1)$, $P_h^r(i+s)$ are the vertical and horizontal projection curves of the right frame. M , N is the vertical rows and horizontal columns at the left frame 1 and the right frame 2. The minimum of $C_v(w)$ is W_v^{MN} and that of $C_h(w)$ is W_h^{MN} , respectively. Then, we can get the motion vectors from the formulas (4) and (5):

$$Tx = S + 1 - W_h^{MN} \quad (4)$$

$$Ty = S + 1 - W_v^{MN} \quad (5)$$

T_x and T_y are the translation (motion) vectors, denoted as offset- x and offset- y . Consequently, we can perform compensation operation to the right frame using two offset values (T_x and T_y).

B. AFFINE TRANSFORMATION MODEL

The change of video image can be divided into translation and rotation. Often, we choose the Affine transformation model. In this paper, we will consider changes of rotation and translation. The angle variable of θ is the rotation parameter in Affine model. From the given left image and right image frame, by adopting Sobel gradient operator [6], we can compute the angle of θ which is rotation parameter at $Y(i, j)$ in the left image frame and right image frame respectively. The two 3×3 templates are used by Sobel gradient operator. Every gray value in the image frame should use these two templates to do convolution. One of the two templates has a maximum response to the vertical edge and the other has a maximum response to the horizontal edge. Then, the Sobel operator can compute the vertical and horizontal edge orientations. We can get the angle orientations for the corresponding formula as follows:

$$\theta = \tan^{-1} \left(\frac{H_v}{H_h} \right) \quad (6)$$

Here, H_v and H_h are the vertical and horizontal edge orientations. The size of the image frame is $M \times N$.

III. ARCHITECTURE AND DESIGN

In this section, we develop an efficient hardware architecture based on the gray-scale projection algorithm and Affine transformation model. In particular, we focus on developing the architecture for stereoscopic image processing. The flow diagram of the computation for luminance (Y) component is shown in Fig. 2. The image processing system is designed to take an 8-bit gray-scale left and right input images. We note that the proposed stereoscopic image processing system can be applied equally well to 8-bit images by simply performing the luminance (Y) operation on the image while skipping the other color format operation. In Figure 2, we need to compute the edge orientation of each pixel of the left and right images at $Y(i, j)$. We set up a table in RAM whose dimensions are equal to input images. Each table entry contains the computed angle orientation for the corresponding pixel of the input images at $Y(i, j)$. Hence, we can calculate the histogram of the angel orientation. Subsequently, we find dominant angle orientation from the histogram. Let H_{\max} denote the number of pixels that has dominant angle orientation in the left and right image

frames. If $H_{max} > \text{threshold}$, then we can obtain the current frame. Then, oriented with direction, H_{max} will be set as the dominant angle orientation. After fixing the dominant angle orientation in the left and right current frames, we can get the difference angle orientation as follows:

$$\Delta\theta(m,n) = |\theta_p(m) - \theta_p(n)| \tag{7}$$

Here, $\theta_p(m)$ and $\theta_p(n)$ are the left and right dominant angle orientations of the current frames, where m, n is the image sequence of the left and right frames ($m, n = 0, 1, \dots, N$).

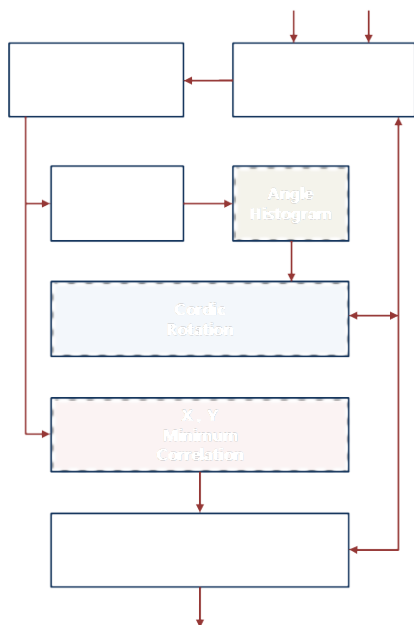


Figure 2. Data flow graph of computation required in motion and rotation vector

After $\Delta\theta(m,n)$ has been computed, we can compute the corresponding difference dominant orientation angle by adopting the CORDIC computing technique [7].

Computations of the rotations are performed using an additional angle accumulator, which is given by;

$$Z_i + 1 = Z_i - d_i \tan^{-1}(2^{-i}) \tag{8}$$

where, $d_i = -1$ if $Z_i < 0$, otherwise $d_i = +1$

In particular, we notice that a small look up table (one entry per iteration) containing the $\tan^{-1}(2^{-i})$ is required for the angle computation. Then, we can get the angle orientation of θ , which is the rotation parameter of Affine transformation model described by section II. So the transformation model can be divided into two parameters of the Affine motion model described in the following formula:

$$\begin{bmatrix} X' \\ Y' \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} X \\ Y \end{bmatrix} + \begin{bmatrix} T_x \\ T_y \end{bmatrix} \tag{9}$$

Here, X, Y and X', Y' are the pixel points in the left image frame and the right image frame respectively. The $\cos \theta, \sin \theta$ are the rotation parameter. T_x is the final horizontal direction motion vector and T_y is the final vertical direction motion vector. After T_x and T_y have been computed, we compensate the current right image frame as shown in Figure. 2. Then, we can achieve the stereoscopic image process.

IV. EXPERIMENTAL RESULTS

In this paper, we respectively compare our proposed architecture with the traditional computing works written by C++ language. The proposed architecture is tested for 6 video sequences. Then, we select one frame image in video sequence as an experimental data, shown as Figure 3(a) and Figure 3(b).



Figure 3. Original Left, Right Image and Result Image (tsukuba)

Similarity can be evaluated by examining the difference between two images. We can get rid of background as well using the difference image. If two frames have movements, the difference image is white. If two images are the same, the difference image is completely black. Figure 3(d) shows the difference image between the left frame and right frame derived from proposed algorithm written in C++ language. Similarly, Figure 3(e) shows the difference image between the left frame 101 and right frame 101, which we implement the proposed algorithm with hardware architecture. Comparing Figure 3(d) and 3(e), the results show almost

identical performance. Several blocks of our proposed algorithm are implemented in Xilinx Spartan -3 FPGA and their parameters are shown in table I. We processed four different videos adopting our new architecture. From table I, we can see that our proposed architecture can achieve real-time processing for various large size of videos. In Table II, comparison between the proposed architecture and other systems implemented by previous authors [8] are shown. From table II, we can see that our proposed architecture has faster speed (frame/s) than SAD based block matching architecture. We can't utilize the identical Xilinx FPGA implemented by D. Chaikalis, et al since our proposed system uses the internal memory block in Xilinx FPGA. Table III shows the resource usage for our proposed system.

TABLE I. HARDWARE IMPLEMENTATION DATA OF VIDEO

FPGA Device	Max (MHz) Frequency	Image Size	Total clock number	Frame /sec
Spartan-3 xc3a5000	51.287	380 x 340	386212	132
		400 x 400	478412	106
		640 x 480	919532	55
		1024 x 768	2355980	21

TABLE II. COMPARISON BETWEEN OUR ARCHITECTURE AND OTHER SYSTEM

Author	Algorithm Used	Platform Used	Frame Size	Frame /sec
Proposed System	- Gray-Scale Projection	Xilinx Spartan-3 xc3a5000	640 x 480	55
	- Affine Transformation Model		1024 x 768	39
N.H. Tan et al	SAD	Altera DE2-70 Cyclone II	640 x 480	35
D. Chaikalis, et al	SAD	Xilinx Virtex XCV-2000E	1024 x 768	31

TABLE III. RESOURCE USAGE OF OUR SYSTEM

Logic Utilization	Used	Utilization
Number of Slices	769	2%
Number of Slice Flip Flops	691	1%
Number of 4 input LUTs	1354	2%
Number of bonded IOBs	157	24%
Number of BRAMs	6	5%

From table I and III, area/throughput estimates based on the synthesis results of a Verilog description of this architecture will be provided to show the feasibility of a single chip ASIC implementation. The peak signal-to-noise ratio (PSNR) between the stabilized frames is an important criterion to evaluate the fidelity of the DIS. The PSNR gives the relation between two frames in terms of their powers.

The higher the PSNR, the better is the fidelity of the DIS. The PSNR between left frame and right frame is defined as [4].

TABLE IV. HARDWARE IMPLEMENTATION DATA OF VIDEO

Image	Size	Frame /sec	PSNR	
Image 1 (tsukuba)	640x480	55	Original Left Image / Original Right Image	17.25
			Original Left Image / S/W Process	20.43
			Original Left Image/ H/W Process	20.41
			S/W Process / H/W Process	43.56
Image 2 (venus)	640x480	55	Original Left Image, Original Right Image	17.39
			Original Left Image, S/W Process	17.42
			Original Left Image, H/W Process	17.80
			S/W Process, H/W Process	20.49
Image 3 (teddy)	640x480	55	Original Left Image, Original Right Image	14.18
			Original Left Image, S/W Process	15.97
			Original Left Image, H/W Process	16.01
			S/W Process, H/W Process	19.06

Table IV shows the PSNR results for three video test images proposed by our hardwired architecture. In comparing three video images(S/W process right image) processed by DIS algorithm written in C++ with the one processed by our hardware architecture, our proposed hardware algorithm shows competitive value of PSNR with less computation time. The gray-scale projection algorithm is known to be inferior because of rough compensation. However, we can take this strategy in favor of reducing the amount of computation time, although there is a disadvantage in terms of the accuracy.

V. CONCLUSION AND FUTURE WORKS

In this paper, we proposed an efficient architecture, which combine gray-scale projection and Affine transformation model. The proposed architecture achieves real time processing speed of more than 30 fps. It is proved that implementation of the stereoscopic image processing system is feasible with the proposed architecture. For further work, it is recommended that our system is investigated more with other algorithm such as 3D tracking and depth Map algorithm.

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