VALID 2017

The Ninth International Conference on Advances in System Testing and Validation Lifecycle

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Forward

The Ninth International Conference on Advances in System Testing and Validation Lifecycle (VALID 2016), held on October 8 - 12, 2017- Athens, Greece, continued a series of events focusing on designing robust components and systems with testability for various features of behavior and interconnection.

Complex distributed systems with heterogeneous interconnections operating at different speeds and based on various nano- and micro-technologies raise serious problems of testing, diagnosing, and debugging. Despite current solutions, virtualization and abstraction for large scale systems provide less visibility for vulnerability discovery and resolution, and make testing tedious, sometimes unsuccessful, if not properly thought from the design phase.

The conference on advances in system testing and validation considered the concepts, methodologies, and solutions dealing with designing robust and available systems. Its target covered aspects related to debugging and defects, vulnerability discovery, diagnosis, and testing.

The conference provided a forum where researchers were able to present recent research results and new research problems and directions related to them. The conference sought contributions presenting novel result and future research in all aspects of robust design methodologies, vulnerability discovery and resolution, diagnosis, debugging, and testing.

We welcomed technical papers presenting research and practical results, position papers addressing the pros and cons of specific proposals, such as those being discussed in the standard forums or in industry consortiums, survey papers addressing the key problems and solutions on any of the above topics, short papers on work in progress, and panel proposals.

We take here the opportunity to warmly thank all the members of the VALID 2017 technical program committee as well as the numerous reviewers. The creation of such a broad and high quality conference program would not have been possible without their involvement. We also kindly thank all the authors that dedicated much of their time and efforts to contribute to VALID 2017. We truly believe that thanks to all these efforts, the final conference program consists of top quality contributions.

This event could also not have been a reality without the support of many individuals, organizations and sponsors. We also gratefully thank the members of the VALID 2017 organizing committee for their help in handling the logistics and for their work that is making this professional meeting a success. We gratefully appreciate to the technical program committee co-chairs that contributed to identify the appropriate groups to submit contributions.

We hope the VALID 2017 was a successful international forum for the exchange of ideas and results between academia and industry and to promote further progress in system testing and validation. We also hope Athens provided a pleasant environment during the conference and everyone saved some time for exploring this beautiful historic city.

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A Method to Determine the Static NBTI Stress Time of an Embedded Component in an Integrated Circuit

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***Abstract*—This paper presents a simple mechanism to accurately estimate the number of clock cycles that an integrated circuit (IC) has operated. It is achieved by measuring the delay of an embedded component due to static negative bias temperature instability (NBTI) effects. Simulations with the HSPICE tool, using 45nm predictive technology model and a NBTI degradation model are presented. The results also indicate that using static NBTI aging model aides in very early stress time detection.**

Keywords-Negative bias temperature instability (NBTI); counterfeit; aging; odometer; built-in self-test (BIST).

I. INTRODUCTION

When a circuit operates, there are changes in certain characteristics which are used in this work in order to determine its operating time. As Complimentary Metal-Oxide Semiconductor (CMOS) technology is shrinking, Negative Bias Temperature Instability (NBTI) was attributed as one of the major causes of changes in circuit characteristics in digital circuits. The NBTI degradation causes an increase in the threshold voltage of a P-type Metal-Oxide Semiconductor (PMOS) transistor and consequently decreasing the transistors drain current and transconductance over time [13]. NBTI is attributed to the creation of interface traps and oxide charges by a negative bias voltage on the gate of the transistor at elevated temperatures. Typically, the stress temperature lies in the range of 100-250°C and the oxide electric fields below 6 MV/cm. Such conditions occur during the burn-in test and normal operation of high performance machines [12]. The threshold voltage of PMOS transistors degrades and this may alter temporal characteristics of a chip.

The focus of this study is to derive an estimate of the number of clock cycles that the integrated circuit (IC) has operated. It is determined by measuring delays due to static NBTI effects. Several models [3][6][14][15][17][18] have been introduced to determine the degradation of the threshold voltage due to NBTI effects. The authors in [17] provide a general framework to analyze NBTI degradation while taking into consideration various circuit parameters like supply voltage, temperature, node switching activity, input patterns, and the duty cycle. The work in [6] introduced an analytical model for dynamic NBTI aging of PMOS transistors based on the Reaction-Diffusion (R-D) model framework. Meanwhile, the authors in [3] and [14] introduced an analytical predictive model for static and dynamic NBTI aging of PMOS transistors based on the reaction-diffusion mechanism of the atoms. They provided an accurate threshold change due to static NBTI aging. However, they only provided upper bounds on the threshold change due to dynamic NBTI aging because the intent was to apply the approach in timing analysis. The authors in [18] presented a framework to analyze the impact of NBTI degradation on circuit performance under various operating conditions such as temperature and frequency. The authors in [2] presented a model to monitor delay on paths in the presence of NBTI aging and process variation. The authors in [7][8][9] considered the effect of hole trapping and interface-state generation to develop an accurate analytical model to identify the threshold voltage degradation due to NBTI. The work in [15] introduced a unified aging model of NBTI and HCI degradation for MOSFET circuits. Their model considers NBTI and HCI effects together to indicate the degradation in threshold voltage at a given time.

This paper presents a built-in approach that estimates accurately the number of operational clock cycles applied to a circuit. In semiconductor industry, an odometer is defined as the instrument used to identify the age of a given circuit. The presented approach acts an odometer as it estimates the number of clock cycles that have been applied to the circuit. The approach operates under static NBTI stress whenever the system clock is enabled. The approach applies static NBTI stress (i.e., low voltage) on the PMOS transistors in a chain of inverters. This causes a change in the threshold voltage of the transistors and subsequently, the delay of the chain of the aging inverters increases rapidly. Static signals are known to age the transistor very fast and therefore the presented approach detects very early stress times. Static signals do not induce dynamic NBTI and Hot Carrier Injection (HCI) effects whose aging effects are not modeled precisely. Hence using static NBTI results into an accurate odometer approach.

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The proposed method is compatible with the IEEE 1149.1 standards and does not impact the timing performance of the circuit. The presented approach will be able to identify the time for which a circuit has been used. This will also help us identify if the given circuit is counterfeit, i.e., has been used in an unauthorized manner.

A counterfeit component is defined as a component which is either an off-specification, defective, or used original component manufacturer (OCM) product sold as ''new'' or working [4]. Recycled components from circuits would operate slower and may fail to work early during their lifetime. Such recycled and remarked components jointly contribute to over 80% of counterfeit products [4]. The reliability of the product is compromised in commercial, industrial or defense applications which pose a major concern in safety critical applications, for example, defense projects and aviation industry. An application of the work is to detect counterfeit integrated chips.

The paper is organized as follows. Section II overviews existing methods to identify aging due to NBTI. Section III provides the preliminaries for the presented work. In particular, it elaborates on the predictive models for static and dynamic NBTI stress. Section IV provides the proposed built-in mechanism and details about the design. Section V provides the experimental results indicating the accuracy of the method in comparison to earlier proposed techniques. Section VI provides with concluding remarks and future work.

II. PRIOR RELATED WORK

There exist some recent NBTI based counterfeit detection methods in the literature. However, all of them rely on dynamic NBTI effects which have not been modeled as accurately as static NBTI effects. It is known that the threshold voltage does not change as rapidly as with static NBTI effects. Instead, the proposed approach uses static NBTI and therefore results into a more accurate prediction of the circuits operating time. Furthermore, dynamic NBTI effects occur concurrently with HCI effects. This complicates their application to the problem studied in this paper.

The authors in [10] consider counterfeit circuit detection without inserting any additional hardware. Two similar circuit paths that undergo dissimilar signal activity are chosen and their delay is calculated with simulations among several circuit instances. The path delays are also computed and curve fitting is done for aged circuit instances. No details are presented on the likelihood of identifying identical paths that are sensitized similarly and there are no details on the signal activity calculation. The latter is a challenging task because the activity on a path depends on the application being executed on the chip. Furthermore, intra-process variations impact the accuracy of the approach. Finding a pair of paths given all the above constraints is a very challenging problem and for some IC's one might not be able to find such a pair of paths. Finally, no results are presented on the total stress time that the PMOS transistors on the paths must undergo during the circuit operation so that the IC stress time is detected.

Another approach for counterfeit detection was recently presented in [11]. The authors use two identical copies of pass logic buffer chains. When the circuit operates, some lines undergo stress at almost every clock cycle. A line with high zero-duty cycle is selected as an input to the buffer chain. The zero-duty cycle was defined as the average time for which a signal remains zero during a clock cycle. This ensures that one of the buffer chains undergoes continuous stress whereas the other chain is kept inactive. The difference in the delays of the buffer chain indicates whether a circuit is aged or not. However, in [11] the authors proposed to take a line from within the circuit. This line needs to have a high zero-duty cycle in the range of 0.9-0.999. It is difficult to find such a line in the circuit. In particular, the zero-duty cycle of a line depends on the application being executed on the circuit. A given line may have the highest zero-duty cycle in a circuit for a specific application but low zero-duty cycle for another application. Hence, it is challenging to identify the line that minimizes the detection of the stress time. Most importantly, we observed that the experimental setup in [11] does not work for circuits that operate at a frequency greater than 1GHz. This happens due to a design flaw. At 1GHz and higher frequencies in particular, the pass logic gate buffers fail to stay open for sufficient time for the signal to cause aging on the PMOS transistor in the chain. This limits the application of the approach. The presented method does not suffer from such challenges.

The authors in [1] present an on-chip NBTI and PBTI tracking technique. Pass logic transistors are used to track dynamic NBTI aging using the model in [3]. The input to the aging sensors is either an internal critical line with the largest duty cycle or a generated signal with similar duty cycle. The objective is to adjust the circuits mode of operation (such as voltage and frequency scaling) as it ages.

The experiments were performed at room temperature but it is known that NBTI effects are pre dominant at high temperatures [13]. Our approach is different than [1] and [11] since we use static NBTI aging. Unlike dynamic NBTI effects, static signals do not cause an increase in temperature due to switching. Therefore, accurate experiments can take place using room temperature. In addition, dynamic NBTI aging is dominated by the duty cycle of the input signal of the aging circuitry which is difficult to calculate [11]. Furthermore, as noted earlier, dynamic NBTI aging should always be considered in concurrence with HCI aging, and neither [1] nor [11] consider the impact of HCI aging effects. For these reasons, [1] and [11] are not good candidates for the odometer application studied in this paper.

The work in [10] and [11] both utilize dynamic NBTI aging, which is explained in the next section. Dynamic NBTI is based on zero-duty cycle which is a very difficult

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quantity to be calculated and the analysis using dynamic NBTI aging is cumbersome. The authors in [5] try to characterize the dynamic NBTI aging effect for different operating conditions. The method utilizes controlled stress conditions. They control the input frequency (in their experimentation, this amounts to controlling the temperature), as well as the zero-duty cycle of the input signal. Furthermore, they control the voltage at which the ring oscillators (ROSC) operate and the time for which the circuit will be aged. Experimental results of manufactured circuits show that dynamic NBTI aging varies greatly as a function of the temperature, even if the zero-duty cycle and other parameters are known. For all these reasons, dynamic aging is not recommended for the odometer problem studied in this paper.

III. EXISTING PREDICTIVE NBTI MODELS

Several NBTI aging models have been presented in the literature, see [3] and [6]. The change in threshold voltage (ΔV_{th}) due to NBTI aging is modeled using the Predictive Technology Model (PTM) in [3]. It is very accurate in modeling static NBTI aging. The static NBTI aging equation is:

$$\Delta V_{th} = A\left((1+\delta)t_{ox} + \sqrt{Ct}\right)^{2n} \quad (1)$$

where t is the total stress time and n is the time exponent, n = 1/6 for H_2 diffusion based model. Let $C = T_0^{-1}\exp(-E_A/kT)$ where $T_0 = 10^{-8}$, $E_A = 0.49\ eV$. Let k denotes the Boltzmann constant, i.e., $k = 1.381 \times 10^{-23} m^2 kg s^{-2} K^{-1}$ and T is the temperature. Let δ = 0.5 and t_{ox} denotes the oxide thickness and is technology dependent. A is given as

$$A = \left(\frac{qt_{ox}}{\epsilon_{ox}}\right)\left(K^2 C_{ox}(V_{gs} - V_{th})\left(\exp\left(\frac{E_{ox}}{E_0}\right)\right)^2\right)^{1/2n} \quad (2)$$

Electric field is given as $E_{ox} = (V_{gs} - V_{th})/t_{ox}$. Let q be the electron charge. Let C_{ox} denote the oxide capacitance per unit area and is expressed as $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{\epsilon_o \epsilon_r}{t_{ox}}$

Let ϵ_o denote the permittivity of free space, its value is $\epsilon_o = 8.854 \times 10^{-14} F/cm$. Let ϵ_r denote relative permittivity and is $\epsilon_r = 3.9$ for SiO_2. Let $K = 8 \times 10^4\ s^{-0.25} C^{-0.5} nm^{-2}$ and let $E_0 = 0.335\ V/nm$

It is observed that under static NBTI stress, the temperature of the transistors does not increase since there is no switching activity. It will be shown that one can accurately estimate the number of clock cycles for which static stress is applied as long as the process parameters such as t_{ox}, V_{th} are known.

For completeness, the section also outlines the predictive model for dynamic NBTI aging, which is used in [5][10][11]. The model provides an upper bound and not necessarily an accurate estimate. The upper bound on dynamic NBTI aging was calculated using the expression below.

$$\Delta V_{ths,m+1} = (K_v^2 \alpha T_{clk})^{2n}\left(\sum_{i=1}^{m}\underbrace{\left(\prod_{j=m-i+1}^{m}\beta_t^{1/2n}\right)}\right)^{2n} \quad (3)$$

$$\Delta V_{ths,m+1} = (K_v^2 \alpha T_{clk})^{2n}\left(\sum_{i=1}^{m}\underbrace{(\beta_t^{1/2n})^i}\right)^{2n} \quad (4)$$

The underlined term in (3) and (4) was estimated as $(\beta_t^{1/2n})^i$ and $\frac{1}{1-\beta_t^{1/2n}}$ respectively which provides the upper bound. It is important to focus on an accurate NBTI aging model since the goal is to precisely identify the time for which the circuit has been used.

$$\Delta V_{th} \leq \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1-\beta_t^{1/2n}}\right)^{2n} \quad (5)$$

The change in the threshold voltage due to dynamic NBTI aging is given by (5) [3]. The dynamic NBTI model considers various parameters to determine the effect on threshold voltage due to NTBI aging namely duty cycle (α), temperature (T), oxide thickness (t_{ox}) and gate to source voltage (V_{GS}) as shown in the equations below. From [11] it was observed that dynamic NBTI aging is very sensitive to α. Calculating α for embedded lines in an IC is a challenging problem.

$$\beta_j = 1 - \frac{2\xi_1 t_e + \sqrt{\xi_1 C(1-\alpha)T_{clk}}}{2t_{ox} + \sqrt{CjT_{clk}}} \quad (6)$$

$$C = T_0^{-1}\exp(-E_A/kT) \quad (7)$$

$$K_v = \left(\frac{qt_{ox}}{\epsilon_{ox}}\right)^3 K^2 C_{ox}(V_{gs} - V_{th})\sqrt{C}\exp\left(\frac{2E_{ox}}{E_0}\right) \quad (8)$$

For these reasons, it is a cumbersome task to use dynamic NBTI aging as a method to predict the number of clock cycles that the circuit has operated.

IV. THE PROPOSED APPROACH

The proposed method inserts two identical chain of inverters in comparison to the pass logic transistors used in [11]. One of the chain ages while the other does not. When a test signal is applied to both chains, the delay difference is measured. This delay is sufficiently large enough that it can be easily detected at a very early time. Then the proposed odometer method uses a pre-determined relation of observed delay vs. static NBTI stress time in order to identify the number of operating clock pulses in the design, i.e., the age of the circuit.

As stated earlier, the proposed approach consists of embedding two inverter chains. One chain will experience static NBTI stress and age rapidly. Let this chain be denoted as AC_s. The other chain will not age and will only be activated during testing. Let this chain be denoted as NAC_s. The delay of the AC_s changes due to the static NBTI when compared to the delay of the NAC_s. This AC_s delay is increasing as a function of the static stress time. A built-in approach that is capable of detecting a delay on the AC_s no less than 12.803ps in 45nm technology with V_{gs}=1.9 V and $T = 300\ K$ is presented.

Then the odometer method is based on Figure 1 which shows the correlation of the AC_s delay to the static NBTI stress time. The relationship depicted in Figure 1 is very accurate for the following two reasons. First, the ΔV_{th} calculation in (1) is very accurate given that the mentioned constants and t_{ox} = $1.3nm$, V_{gs} = $1.9\ V$ are used. The t_{ox} is technology specific and V_{gs} is decided by the designer hence these values can be easily extracted. Secondly, there are mainly two process parameters that may affect the accuracy namely the oxide thickness t_{ox} and temperature T. Since the use of static NBTI stress, the approach is unaffected by the temperature. For t_{ox}, using simulations, it has been verified that the change in ΔV_{th} is very negligible to cause any significant deviation from the ideal inverter delay shown in Figure 1. Thirdly, there are other fabrication parameters that might cause variations but the two inverter chains are so closely placed, such that those variations will cancel out and will not affect the accuracy of the presented approach. Even though the work in [10] was unaffected by intra-die process variations, it was not immune to the process parameters t_{ox} and T.

When a circuit is activated the clock is applied to the respective module of the circuit based on the application executed on the chip. Hence, a circuit has been aged for as long as the clock is applied. Thus, it is proposed to use the clock signal to monitor the age of the circuit. It is known that static NBTI aging causes the most rapid degradation in the threshold voltage. Hence, the proposal is to generate a static zero signal using the clock of the circuit.

A combination of an AND gate (G2) and an inverter (G1) is used as shown in Figure 2. The system clock signal and its inversion are given as input to the AND gate. Due to the AND gate properties, a constant zero signal is generated. The delay introduced due to the inverter causes very small glitches in the generated signal. The glitches do not reach sufficiently high voltage to switch the state of the transistor. Hence, the glitches are not a problem and the transistor is constantly stressed.

This static zero signal will be an input to stress time detection module (STDM). The STDM consists of two

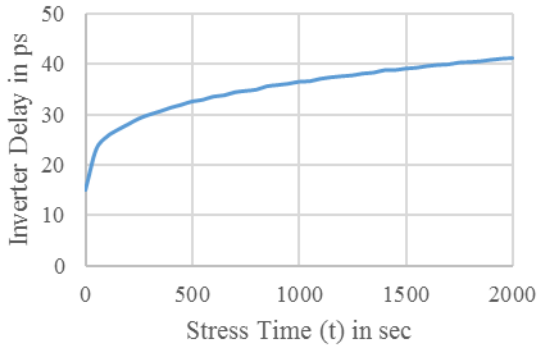

Figure 1. AC_s detected delay due to applied static NBTI stress.

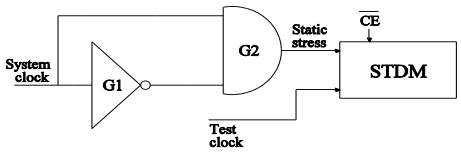

Figure 2. Static zero generation using system clock signal.

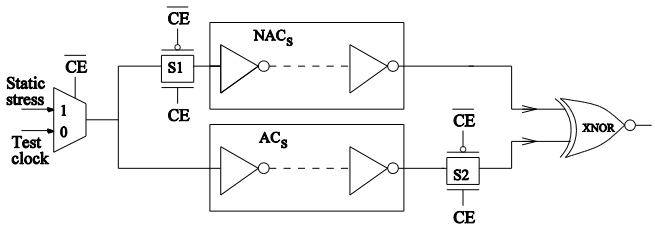

Figure 3. The schematic of STDM.

similar chain of inverters embedded on the chip which are placed very close to each other as shown in Figure 3. Hence, the two inverter chains are unaffected by intra-die process variations. One of the inverter chain experiences static NBTI stress. Let us call this chain as Static Aging Chain (AC_s) while the other is only enabled during the testing phase. Let us call this inverter chain as Static Non-Aging Chain (NAC_s). There is a multiplexer to control the input to the two the NAC_s and AC_s chains. The multiplexer during normal operation of the IC lets the static signal through and lets through the test clock during the test phase depending on the current mode of operation controlled by circuit test enable signal ($\overline{CE}$). There is a XNOR gate to detect the delay between the NAC_s and the AC_s. During the normal operation of the circuit, the NAC_s is isolated from aging using a pass logic transmission gate S1 meanwhile S2 isolates the XNOR from aging.

During normal operation of the circuit, $\overline{CE}$ is 1. Thus, switches S1 and S2 are closed and the static stress input only ages the AC_s. Meanwhile, the NAC_s is not aging at all. During the test mode, $\overline{CE}$ is switched to 0 hence, the test clock signal is applied to the STDM. This test clock signal can be chosen as the system clock or any signal as per the designer. During experimentation, it was assumed as the system clock. Since $\overline{CE}$ is now 0, the switches S1 and S2 are open and the test clock signal is applied to the NAC_s and AC_s. This signal propagates through the two chains. The NAC_s signal is going to arrive earlier than the AC_s signal due to the aging induced in the AC_s. The XNOR will identify the delay between the two chains and produces a pulse proportional to the delay between NAC_s and AC_s. This pulse can be observed at the output pin of the chip. There are many techniques in the literature that can be used to detect on-chip delay of paths for example [16]. But having a dedicated pin will help us provide more information about the chip in the future.

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V. EXPERIMENTAL RESULTS

Experimental results have been evaluated on some of the largest ISCAS'89, ITC'99 benchmarks. Experiments were conducted on a Linux machine with Intel Xeon 6 core @ 2.40GHz processor and 23GB memory. The first transistor in the chains is minimum sized. The PMOS size is $(W/L)p=(0.24U/0.045U)$, while the NMOS size is $(W/L)n=(0.12U/0.045U)$. Successive inverters are sized using appropriate sizing techniques. HSPICE [20] simulations are performed by using predictive PTM 45nm technology library [19].

Firstly, the experiments were performed using a single inverter, which experienced static NBTI aging. The PMOS and NMOS sizes used for this inverter are as mentioned above. The earliest detection time for static NBTI stress was found to be 30 days which is an unreasonable static NBTI stress detection time. To facilitate a much earlier detection, an inverter chain consisting of 100 inverters was used. It was necessary to use such a substantial number of inverters because only half of the inverters will be stressed. This is due to the inversion of the signal and the fact that NBTI aging occurs only on the PMOS transistors.

The experiments were repeated and it was found that the earliest detection time using the 100 inverter chain was reduced from 30 days to 2 seconds. The corresponding delay was observed to be 12.803ps. One can either choose an earlier detection time or reduce the hardware overhead and have a late detection time. But choosing a later detection time may leave your IC's integrity vulnerable.

Experiments were performed on some of the important benchmarks. The ISCAS'89, ITC'99 benchmarks were used in order to compare the results of the presented approach to [10]. Table I lists the earliest detection time for the proposed approach and [11] with different zero-duty cycle (ζ) observed for the known ISCAS'89, ITC'99 benchmarks. The work in [5] was excluded from the comparison below since it does not work for high frequency circuits and the work in [10] since it does not calculate the earliest stress detection time. Column 1 lists the approaches and various ζ values for [11]. Column 2 in Table 1 lists the earliest detection time observed for the two approaches. Column 3 lists the benchmarks which have the property of having a single line with the ζ mentioned in Column 1.

In particular, row 1 shows that the earliest detection time for static NBTI aging is 2 seconds. This detection time holds for any given circuit because the proposed approach is based on the static NBTI stress generated using the system clock. Row 2 presents the earliest detection time for the approach using [11] and ζ=0.997. Using input zero probability 0.5 and simulations showed that the circuits b15 and s15850 from the ITC'99 and ISCAS'89 collections, respectively, have a line with ζ approximately 0.997. Thus, the earliest detection NBTI stress time for each of these two circuits is approximately 72.3 hours.

The improvement over [11] becomes even more pronounced for circuit b20 from the ITC'99 collections

TABLE I. COMPARISON OF EARLIEST DETECTION TIME FOR BENCHMARKS USING PROPOSED APPROACH AND [11]

		Earliest Detection Time	**Benchmarks**
Proposed Approach		2sec	Any
[11]	ζ=0.997	72.3h	b15, s15850
	ζ=0.984	504h	b20
	ζ=0.981	528h	b22
	ζ=0.977	674h	s13207, s35392

where the ζ is 0.984 Column 2 shows that the earliest NBTI stress time detected using [11] is 504 hours. Likewise, it is observed that the impact of the method for circuits b22 is much more pronounced. For this circuit, the simulations showed that the ζ is 0.981 and the earliest detection time was found to be 528 hours. Meanwhile, for s13207 and s35392 the ζ was found to be 0.977 and the earliest detection time was found to be 674 hours. All these results show that the proposed approach is significantly better among the two.

Adding 200 inverters might seem like a huge hardware overhead hence a simple study to identify the hardware overhead was performed. The total number of transistors for the ISCAS'89, ITC'99 benchmarks reported in Table III were calculated using the transistor count of individual gates and flip-flops present in the benchmarks. Table II lists the transistor count of the different gates present in the reported benchmarks. Column 1 lists the type of the gate or component. Column 2 lists the number of transistors present in the respective gate or component.

Table III lists the hardware overhead of the proposed approach on select ISCAS'89, ITC'99 benchmarks. Column 1 lists the benchmarks that were used to measure the hardware overhead. Column 2 provides the total number of transistor in the given benchmarks. Column 3 lists the overhead percentage of the proposed approach. It is observed that the hardware overhead of the complete approach is less than 0.54% for some of the biggest ITC'99 benchmarks. Even for the smaller benchmarks like b15, s15850, and s13207, the hardware overhead is less than 1.26%. This proves that the proposed method provides a significant improvement over existing approaches as well as minimizes the hardware overhead for such a challenging problem formulation.

TABLE II. TRANSISTOR COUNT FOR VARIOUS LOGIC GATES

Logic Gates	**Transistor Count**
D Flip Flop	18
AND, OR	6
NAND, NOR, BUFFER	4
INV	2

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TABLE III. HARDWARE OVERHEAD OF THE PROPOSED APPROACH

Benchmarks	Total number of transistors	Overhead (%)
s13207	36646	1.26
s15850	41900	1.1
b15	42396	1.09
b20	86340	0.54
s35392	98138	0.47
b22	128600	0.36

VI. CONCLUSIONS

A method for the earliest identification of the delays due to static NBTI stress is proposed. The approach uses inverters that age at each application of the system clock. The experimental results show that the approach detects static NBTI aging very early in the lifetime of a circuit. The method can be used as an odometer for the life cycle of the circuit independent of its operating frequency. The approach has negligible built-in hardware overhead.

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Application of Extended Timed Automata to Automotive Integration Testing

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Abstract— **Deployment of the Model-based Testing methods in practice has not achieved the level it deserves. To help dissemination, as well as to improve the testing process in a particular domain, this paper presents a new Test Generation tool on a case study. The domain is automotive integration testing. The new tool is named Taster and utilizes Timed Automata for the online Model-based test generation. The objective of these tests is testing of integration of automotive comfort systems. The proposed concept, the system modeling, and the new software tool is evaluated on testing of a Keyless Access System. Purpose of the paper is to present an approach for automatic test generation intended for automotive integration testing.**

Keywords- Model-Based; Integration; Testing; Timed; Automaton; Automotive; ECU

I. INTRODUCTION

This paper presents an application (new tool implementation) of Model-Based Testing (MBT) approach to the integration testing of automotive electronics systems - i.e. a cluster of Electronic Control Units (ECU). In current practice, the original test suite is developed by test engineers as a sequence diagrams. The test suite development is labor intensive, and amount of work should not grow in future. On the other hand complexity of automotive systems still grows. Test suite complement in the form of automatically generated test cases is offered, to keep the amount of test development works reasonably.

The key idea is to supplement a test suite developed traditionally by a test suite generated using the MBT principles. These additional test cases are generated by a software tool called Taster. MBT process is driven by a Timed Automata model. One of the limitations of traditional test suites is that test cases are designed using driver-oriented point of view. One of the goals of presented work is to overlook from this narrow use case and, using the MBT techniques, to produce traces, which examine system by more diverse, but still reasonable stimuli. In other words, we presume that usefully complement test suite created by engineers with machine-generated ones can significantly increase the number of revealed faults. The proposed solution is evaluated on a short case study with the objective to judge the suitability of the developed test generation tool Taster for future research. The proposed solution is depicted in Fig. 1. A short overview of related work follows.

Many model checkers or formal verification tools are based on the Theory of Timed Automata. Also, there are at least hundreds of Timed Automata variants [1]. Usage of this theory for testing is less common than for model verification. TRON [2] and CoVer [3] from the UPPAAL connected tools family are probably the most relevant research for presented approach. Both tools use the UPPAAL model checking engine for the test generation. Presented tool Taster uses a different technique. It uses own algorithms based on graph search theory. Taster tool evolves on a basis of our conceptual work [4]. This paragraph is focused on Timed Automata linked works. Besides introduced tools, RT -Tester [5] can be mentioned as it is targeted to similar SUT class. RT-Tester uses a subset of UML or SysML as modeling format.

Paper is organized in following structure. Section *II* describes the problems of the current practice of integration testing in more details. Section *III* shows overall testing concept and system modeling - Timed Automata model with an extension. In Section *IV* are presented algorithms developed for the test generation and our test generation tool Taster. Section *V* contains the Keyless Access System (KESSY) case study, which is subdivided into four subsections. Last two sections are Conclusion (*VI*) and Future work (*VII*).

II. PROBLEM STATEMENT

Consider an automotive integration testing scenario. For a System under Test (SUT), a test suite based on the test plan is developed. This test plan covers demands from compulsory road regulation, internal standards, and a system specification. The specification is usually created and maintained by requirement management software (e.g., Rational DOORS). An SUT is tested using black box approach – no internal structure or similar information is employed to test suite design. All test cases are developed from a driver point of view (a typical driver use case). The testing process itself is driven by EXAM [6], which covers tasks from individual test case implementation to management, execution, and assessment of complex test suites. Despite careful and hard testing work, it is not possible to cover all possibilities by a manually developed test suite. The reason is in the system complexity and associated well-known State space explosion problem [7] together with limited time and cost resources.

In this process, various improvement possibilities can be identified. First of all, manual development of the integration tests manually is very labor intensive. Therefore, decreasing of a size of original test suite in behalf of automatically generated one should be significantly beneficial. Also, complementing the suite by test cases developed differently

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could help achieve better test diversity. This work addresses these challenges by the development of an MBT test tool able to operate with an SUT controlled by EXAM.

III. CONCEPT AND SYSTEM MODELING

Overview of proposed concept is depicted in Fig. 1. The textual specification is presumed as the basis for the model development. SUT is modeled as a network of Timed Automata. UPPAAL [8] is used in the role of model editor. Complete testing is driven by this model – no other models or configuration files are used.

Figure 1. Concept of implemented solution

Taster tool explores the models using graph theory algorithms. Test inputs are produced online, and the SUT outputs are checked against expected ones. The model simulation is directly used for test generation. The algorithms are described in detail in Section *VI*. Interaction with an SUT is done by NI VeriStand or EXAM test adapter.

The proposed solution employs UPPAAL tool [8] as a modeling environment. The system is modeled as a network of Timed Automata. The underlying theoretical concept is denoted Timed Safely Automata. Beyond theoretically described [1] time and transition properties, the UPPAAL implementation offers usage of variables, conditions, synchronization channels and another language construct to provide a certain level of expressivity (in theory summarized by term action). The used modeling language is a subset of UPPAAL modeling language summarized in Tab 1.

TABLE I. SUPPORTED SUBSET OF UPPAAL MODELLING LANGUAGE

	Action		
Data type	**Guard**	**Update**	**Sync**
clock	✓	reset	×
chan	×	×	✓
bool	✓	✓	×
int	✓	✓	×

The subset is chosen concerning tested system class. Supported data types are *bool*, *int*, *clock* and synchronization type *chan*. Edges can contain *guard*, *sync*, and *update* expressions.

Besides Timed Automata modeling language implemented by UPPAAL tool, Taster additionally utilizes labeling of Timed Automata states by relevance. *Relevance* is a natural number assigned to an automaton state. The parameter expresses the importance of a model state summarized by one number. The higher value implies the higher testing priority. *Relevancies* are assigned according to the SUT expert knowledge. It is determined in a manual or automatic way and originates in for example safety impact, the impact on rest of the system operability, and previously revealed issues (bugs). KESSY testing example presented later in this paper shows usage of *Relevancies* on environment models of start and door buttons.

The success of proposed solution strongly depends on the reasonability of used model. In this work, two types of models are used. The first category is environment Models, which produces inputs for an SUT during simulation. The second category is observer models which have the Oracle function – they check expected SUT outputs. Correct output is expressed as an invariant condition. SUT behavior is considered valid if invariant in an active state is satisfied. The division of the model into environment and observer parts is only imaginary, and it is possible to combine input and output actions to single Timed Automaton. Nevertheless, partitioning of entire model to these two model types is recommended to keep clarity.

IV. ALGORITHMS AND TOOL

The test generation is based on the model exploration using graph search techniques. Timed automata model is simulated in a Real-time. The SUT input and outputs are linked to the model variables. Consequently, variable assignment on model edges produces test stimuli. The SUT outputs are observed using variables utilized in location invariant conditions. The progress of the time is discrete, and it is equal to the time of simulation step. Developed algorithms are described in pseudo code. The first algorithm (Fig. 2) describes the overall testing process.

```
Algorithm 1
DoTesting (Model):
  while invSatisfied and covCritNotSatisfied
    ReadInputs
    DoStep (Rand. | Prized R. | Sys.)
    UpdateClocks
    WriteOutputs
```

Figure 2. Algorithm 1

Three different strategies are used to choose next step (i.e. edge to be taken). First step common for all strategies is the creation of a list of allowed edges in that time. Allowed edge is an edge with satisfied guard condition. If the edge triggers synchronization, corresponding edge waiting for synchronization has to be allowed. In case the list of allowed edges is empty, no edge is taken, clocks are incremented and the loop continues to next iteration. The loop is stopped if the invariant is violated, coverage criterion is satisfied, or test is stopped by the test operator. Algorithms 2 and 3 take next edge randomly from the list of allowed edges. Algorithm 2 (Fig. 3) works with discrete uniform distribution – probability of pickup is the same for all edges in the list.

```
Algorithm 2
DoStepRandom (Model):
for each ActiveNode in Mod. Templates:
  for each OutEdge in OutEdges:
    if GuardIsSatisfied(OutEdge)
      listOfAllowedEdges.Add(OutEdge)
nextEdge = Rand(listOfAllowedEdges)
```

Figure 3. Algorithm 2

Algorithm 3 (Fig. 4) modifies discrete uniform distribution using *Relevance* numbers defined in the previous section. Probability of taking for an edge *i* from the list of allowed edges is:

$$P(E_i) = \frac{rel_{E_i}}{\Sigma rel_E} \quad (1)$$

Implicit *Relevance* is equal to one. *Relevance* is assigned to an edge from its target node. It may be confusing, but reason is to preserve compatibility with UPPAAL model format. *Relevance* is stored as a node comment, which is not possible with an edge.

```
Algorithm 3
DoStepPrioritizedRandom (Model):
for each ActiveNode in Mod. Templates:
  for each OutEdge in OutEdges:
    if GuardIsSatisfied(OutEdge)
      listOfAllowedEdges.Add(OutEdge)
nextEdg = PrizedR.(listOfAllowedEdges)
```

Figure 4. Algorithm 3

```
Algorithm 4
DoStepSystematic (Model):
for each ActiveNode in Mod. Templates:
  for each OutEdge in OutEdges:
    if GuardIsSatisfied(OutEdge)
      listOfAllowedEdges.Add(OutEdge)
nextEdge =
PickLowestTakenEdg(listOfAllowedEdges)
```

Figure 5. Algorithm 4

Algorithm 4 (Fig. 5) refers edge with the lowest takes count from a list of allowed edges. Model exploration is more deterministic than in the case of the random strategy. This behavior may speed up structural model coverage if it is desired. Concerning black box testing approach only, the model coverage criteria are feasible. Condition `coverageCriterionNotSatisfied` unify coverage of all Timed Automata model nodes or edges.

The proposed concept with the MBT theory and algorithms results in the implementation of a testing tool named Taster. The first version of this tool was implemented in [9]. Taster works with models stored in UPPAAL 4 format. After a model is loaded, it is possible to performed testing as proposed. The SUT is connected by a test adapter. In following sections, the Taster is described in the order same as testing workflow. First is the model parser and last is the result viewer. The code is written in C# using .NET Framework 4.5.

The software architecture is divided into the model parser and the test execution part. First part is responsible for syntactical check and data structures preparation. Second part implements testing engine itself. The execution part also contains trace logger with replay function.

Syntactical analyzer code is generated by language recognition software ANTLR [10]. Expression evaluation is solved by Shunting-yard algorithm [11]. Syntactical analyzer code is generated by language recognition software ANTLR [10]. Expression evaluation is solved by Shunting-yard algorithm [11]. Traces are stored in an XML file for further analysis.

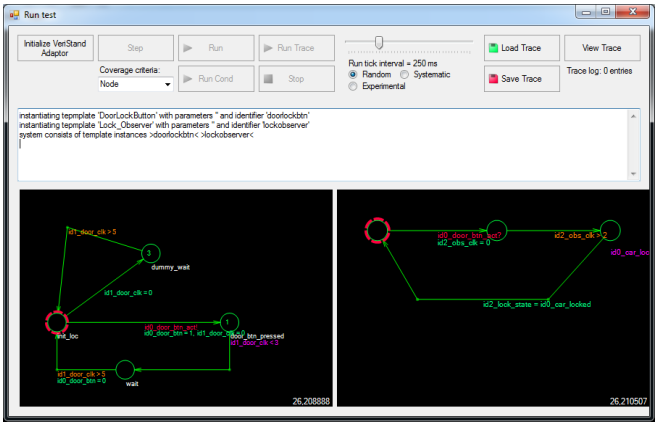

Figure 6. Taster – Test Execution and Control

The usage of the testing tool is displayed in Fig. 6. First is screen (not depicted) is the model viewer where a model is loaded. Second screen is the run screen. On the run screen the test adapter is initialized and a test run is executed according to selected algorithm. A test run is terminated by one of the following actions: invariant is violated, coverage criterion is satisfied, and the test time has passed or by termination by a user request.

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V. KESSY SYSTEM TESTING

The following example shows the application of presented concept on testing of a keyless access system. As the name suggest, the purpose of keyless access system is to allow vehicle entry and engine start without using a key (only the key's RFID tag have to be detected).

A. Specification

The example system function (i.e. textual specification) is captured by this description. The door locking system is controlled by the lock button built in the driver side door handle. The Start/stop button works as the ignition switch. The short press is designated to turn the ignition on and button long press is the command for engine start operation. Button press longer than one second is considered long. Ability to lock and unlock the door, as well as start or stop the engine, is determined by detected key position. The system contains two equal keys RFID tags marked Key 1 and Key 2. The system recognizes following states of each key: detected outside the car, detected inside the car and not detected. The door unlocking is not possible if no key is detected outside the car. The door locking is not allowed if a key is detected inside the car. The engine start requires a key to be detected inside a car.

In modern Vehicles, the KESSY system is implemented as distributed system. Let's consider a system composed from three ECUs. First ECU is the KESSY system itself which cooperates with a Body Control Module (BCM) and Engine Control Unit. All ECUs are interconnected by a Controller Area Network (CAN) bus. The KESSY ECU is responsible for keys and button status monitoring. Based on its commands, the BCM controls power supply system and individual door locks. Engine start and stop procedure are driven by the ECU. The system inputs are described in the previous paragraph. The system is observable by four digital outputs. Door locking system has locked and unlocked states. Start button controls ignition system which controls three power supply branches. German language prefix Klemme (KL) for individual clamps is preserved as, it is standardized by DIN 72552 standard and ISO equivalent does not exist. The system controls KL 15, 50 and S. KL 15 is active if the ignition is on. KL 50 is active during engine startup only and in this work it is used for engine start monitoring. KL S is turned on by switching the ignition on, and it is active until the car is locked. Its common usage is for audio system powering.

B. Models

The example system is modeled by the network of nine Timed Automata. Every system input is modeled by a single automaton. The KESSY system provides two functions – ignition switch controlled by Start/stop button and door locking system control. Correct behavior of each is observed by separate automaton. The relation between keys position and corresponding system behavior is modeled by another three automata. Overall characteristic of the model is stated in Tab. 2.

TABLE II. KESSY MODEL SUMMARY

Entity	Count
Templates	8
Instances	9
Nodes	30
Edges	39
Clocks	7
Variables	15
In/Out variables	6

Due to limited paper range, only Start/stop button model and one of two observer models are described. The first model, the start/stop button, is depicted in Fig. 7. In the case of the Start/stop button, the long and short press are distinguished, in opposite to the door lock button, which has two states only (press and release). Models also contain auxiliary wait states which are used for simulation of user inactivity. Labeling the automaton states by *Relevance* parameter is used for preferring inactivity (wait state) against button pressed. Similarly, it is favored short press before the long press.

The most important parts for distinguishing between expected and incorrect SUT reactions are observer models. Our example uses two observers. Locking System Observer and Ignition System Observer, which is shown in Fig. 8. The system behavior is checked by location invariants. Variables in invariant conditions are mapped to the system outputs. Observers are synchronized with button handling models by synchronization channels.

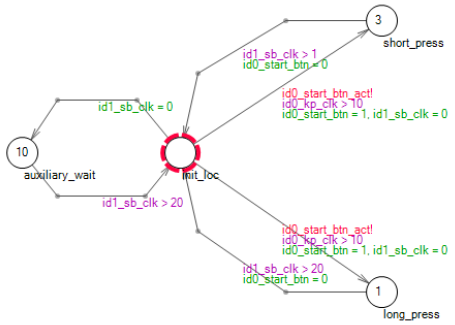

Figure 7. Start button model

A set of simple models capture relation between keys position and allowed system behavior. A key location determines whether it is possible to unlock, lock and start the car. The models produce corresponding signals to handle this situation.

C. Implementation

The experimental SUT was developed using NI VeriStand Real-Time Testing Software. This platform was chosen on the basis of previous experience during development of an HIL test place with our industrial partner. Real KESSY ECU was replaced by an own implementation, as fault injection is much less complicated in its case.

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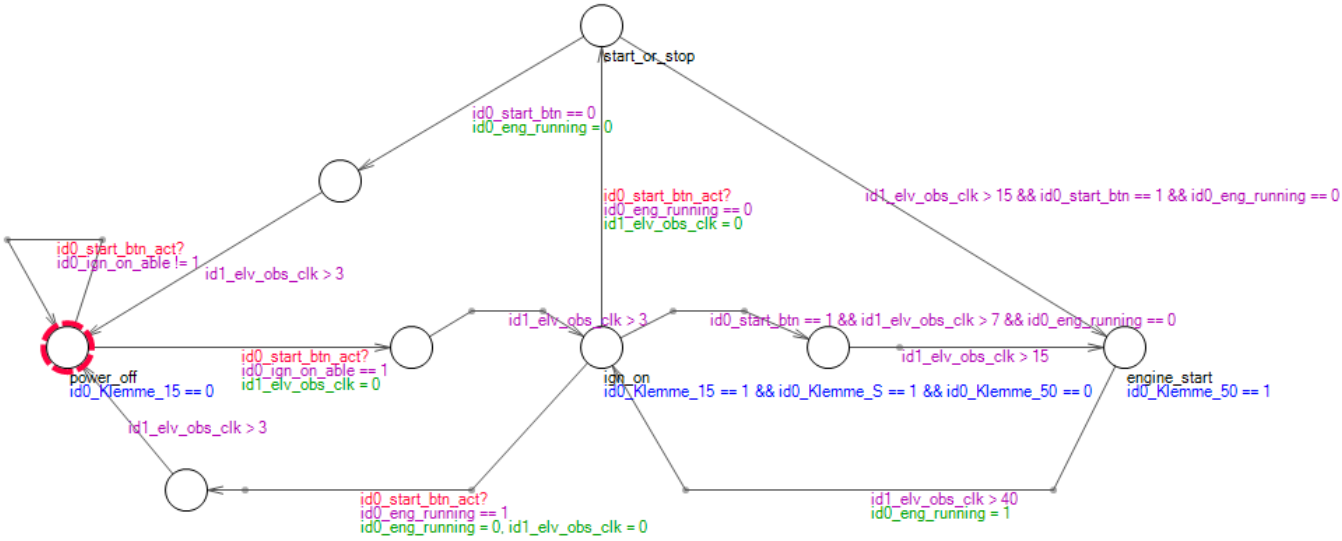

Figure 8. Ignition System Observer

KESSY system, described by specification in Section *VIII.A*, is implemented as three simulation models executed by NI VeriStand Real-Time engine. Partitioning of the SUT into multiple models better reflects distributed nature of a real automotive system. Communication between models is realized by VeriStand channels. The connection of Taster tool to the SUT is done by test adapter which uses VeriStand .NET API [12].

D. Results

Example KESSY system specification was implemented in LabView as VeriStand simulation models and modeled in UPPAAL using Taster supported language constructs. The implementation was afterwards tested by the Taster. Test step period was 100 ms and frequency of the Primary Control Loop of VeriStand was 50 Hz. The objective of the first set of tests was an error detection capability and it was evaluated by injection of three independent faults into SUT.

Fault 1: KL S goes off after 2s from turning the ignition on.
Fault 2: Short start button press is not recognized while the ignition is on – it is not possible to shut down the ignition.
Fault 3: Car is not able to be locked if both keys are detected outside the car.

Faults were injected by modification of implementation models. All inserted faults were successfully detected. Detailed results are summarized in Tab. 3.

TABLE III. KESSY - FAULT INJECTION RESULTS

Fault	Detected	Time to detect	Trace steps	State of detection
F1	✓	39s	392	ign_on
F2	✓	28s	276	power_off
F3	✓	99s	992	check_locked

Detection time is lengthened by key position templates; they wait for arbitrary time quanta between key position changes. Fault 1 and 2 needs at least one key inside the car to allow switching ignition on. Otherwise, the fault is not detectable. Fault 3 is exposed if Key 1 and 2 detected outside the car. Optimization for time or step count is possible in future work and was not objective of presented work. Algorithm 2 – Random strategy was used for fault detection experiment.

Correct implementation was evaluated by performing nine test runs summarized in Tab. 4. No fault was revealed. Node coverage of complete model was selected as stop condition. The SUT model was not optimized for the fastest possible node coverage.

TABLE IV. KESSY – OVERVIEW OF PERFORMED TEST RUNS

Trace	Strategy	Test Time [s]	Steps	Lock state change	Engine Start-Stop
TR 1	Random	45	446	2	2
TR 2	Random	46	458	10	1
TR 3	Random	195	1950	57	2
TR 4	Relevance Random	152	1525	43	1
TR 5	Relevance Random	36	363	1	1
TR 6	Relevance Random	84	841	25	2
TR 7	Systematic	300*	3005	78	9
TR 8	Systematic	300*	3002	78	9
TR 9	Systematic	300*	3004	79	9

*test run was terminated after 300s because it is not possible to reach node coverage

The testing ability for the specific SUT is expressed by a number of locking state changes and engine start and stop cycles included in a test trace. If these two features are examined, the major part of SUT functionality is tested, because they are conditioned by the correct reaction to key position and door and start buttons. Test runs that use Algorithm 4 (systematic) discovered impossibility to achieve node coverage. The reason is in demand of generation of two short start button presses in a row, which is not possible with systematic exploration. Without two consequent short presses, it is not possible to test switching ignition on and off without engine start.

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VI. CONCLUSION

New practical approach to the Online MBT test generation based on the simulation of Timed Automata based model is proposed. The suggested method utilizes well-known Timed Automata formalism as system description language. Test traces are generated directly during the model simulation. Model is simulated by randomized exploration. Testing stimuli are produced by variables included in the model and connected to an SUT by a test adaptor. Correct tested system behavior is checked by invariant conditions. Three variants of exploration algorithm are presented. The proposed concept is implemented as a part of MBT tool Taster. The implementation utilizes UPPAAL tool as model editor and uses a subset of UPPAAL modeling language in UPPAAL 4 file format. On the other hand, *Relevance* parameter coupled with nodes was defined to allow prioritization of certain part of the state space. The target application is the testing of comfort part of vehicle electronics systems, such as door locking, exterior/interior lighting, and air condition. Test adapters for NI VeriStand and EXAM were implemented for connection to a testbed. A case study on a KESSY system was done to validate expected Taster capabilities. Results are promising and indicate the suitability of presented approach for automotive testing application. Last but not least, utilization of UPPAAL models allows performing formal verification besides the testing for the specific part of the SUT.

VII. FUTURE WORK

Presented work can be viewed as a basic step or creation of background for future research in the area of automotive integration testing. Implementation of proposed concept had to address many challenges. The range of performed works was too broad to addressed individual problems thoroughly. Further work is planned to be much specific. In the following paragraphs, two of these specific objectives are outlined.

Described solution is presented as a complement to the original test suite. Let's presume it is developed in EXAM. Both suites should not contain similar test cases. The question is how to algorithmically analyze Taster test runs and EXAM test cases in a comparable way. Comparison of the content of Timed Automata traces with sequence diagrams, or underlying Python code will be useful for assurance of required diversity between Taster and EXAM test cases. Solving of this problem is necessary for the truly synergic effect of the deployment of presented Taster tool beside human developed test cases.

The concept of labeling of Timed Automaton states by *Relevancies* numbers was proposed in System modeling section. In this work are these number assigned manually by an expert knowledge. This concept could become powerful with a machine extraction of the *Relevancies*. Source of information could be some test hypothesis or test results database.

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Improvement of Sequential Tests in IEC-61124 Reliability Testing – Compliance Tests for Constant Failure Rate

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***Abstract* — An improvement of IEC-61124 in the field of a sequential probability ratio test (SPRT) is proposed. The current standard does not provide a proper solution for modern industry's needs, and the test plans are not up-to-date with the knowledge in the area of sequential tests. The advantages of the proposed version are reflected by the efficacy and accuracy of the tests, the wider range of the ready to use test's parameters, and available data regarding the test's characteristics. The proposed version is a significant improvement over the existing one. The changes will extend the use of SPRT and this standard. The proposal for updating the standard has been accepted to the work-plan of TC-56 of IEC.**

Keywords — Exponential distribution; compliance; mass-production; reliability; sequential probability ratio test.

I. INTRODUCTION

The main purpose of the work is to improve the standard IEC 61124 [1] in the field of sequential tests [2]–[5]. Sequential tests have significant importance and actuality in quality assurance and reliability [6] [7]. Today's methods and computing tools permit better planning of sequential tests, in accordance with the latest practical demands (more stringent over time) [8]–[17].

The proposed version will include shorter tests (more economically efficient), more accurate tests, a wider range of test plans, and significant additional characteristic data. It will also address the complex and stringent needs of today's industry.

The sequential method of testing is described as follows. A rule is given for making one of the following three decisions at any stage of the experiment: (1) to accept (2) to reject (3) to continue the experiment by making an additional observation. The process is continued until either the first or the second decision is made.

An essential feature of the sequential test is that the required number of observations depends on their outcome and is not predetermined, but a random variable. Advantage of the sequential test lies in the fact that its expected accumulated test time to decision (ETT) is minimal at two typical points of its operating characteristic (OC) representing the error probabilities of the I- and II-types (α and β) [3] [4].

The characteristics of this test are obtainable from its boundaries [8] by means of Aroian's [18] well-known direct method, following an idea outlined earlier by Barnard [19].

II. MOTIVATION

Sequential tests have a significant importance and actuality in industrial acceptance sampling, in information technology and in reliability examination. The improvement is manifested in the means of the range, truncation and ETT, accuracy, user interface, usability, and in the simplicity of the planning. Accurate data for the test characteristics are part of both today's needs and ability.

A. Disadvantages of the current standard

The standard does not provide a proper solution for modern industry's needs, and the test plans are not up-to-date with the knowledge in the area of sequential tests.

- General:
  - Insufficient range of the test parameters (risks and discrimination ratio). Only a total of 17 "ready to use" sequential test plans are given.
  - The test's truncation is not optimal and considerations for truncation are not homogenous.
  - Lack of information for the relationship between the test truncation time and the expected test time.
  - The method for presentation of the tests (figures and detailed tables in Annex A and D) are suitable only for a few tests (not suitable for many). It limits the number of tests to be displayed in the standard.
  - For some of the test plans (A.4, A.7, A.9, C.8) in the figures of the "accept and reject" lines Y- axes shows non-integer values for the observed number of failures. This is an editorial error.
- Test plans A.1 – A.9:
  - The true producer's and consumer's risks are wrong and far from the nominal.
  - Non-optimal truncation - tests with lower maximum duration and lower expected time are available.
  - Tests are limited to three equal nominal risks only (10%, 20% and 30%).
  - Additional test plans can be calculated by formulas (given in Annex E). The formula leads to substantial deviation (unknown) from the nominal risks and does not carry out optimal truncation.

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- Test plans C.1 – C.8:
  - Non-optimal truncation - the tests are overly truncated, and as a result, have high expected time, so that the sequential tests' advantages are lost.
  - The plans are limited to eight tests with D=1.7 only.

The standard does not provide the needs of modern industry, and the test plans are not up-to-date with the knowledge in the area of sequential tests.

B. Advantage of the proposed version

The proposed version will address the complex and stringent needs of today's industry. It will bring to the fore the latest knowledge and methods in truncated sequential tests.

1) The tests are substantially truncated (the maximum test duration is low) without significantly increasing the ETT [8].
2) The true producer's and consumer's risks are given and always very close to the nominal.
3) A wider range of the test parameters (risks and discrimination ratio) are given—a total of 60 tests.
4) The test plans include a series of unequal risks for producer and consumer.
5) Five accurate values of ETT are given in the test plan table for fulfilling all practical needs (easy to use with spreadsheet for full test characteristics presentation).
6) Suitable for interpolation by risks.

The proposed version addresses the complex and stringent needs of today's industry. It brings to the fore the latest knowledge and methods in truncated sequential tests.

III. DEMONSTRATION AND COMPARISON

This section deals with the examination of the standard's sequential test plans. The analysis included accurate calculation of the true characteristics of the tests A and C. In order to perform the comparison, corresponding test plans were calculated by using the advanced methodology [8]. The comparison focused on the differences in the parameter values (and accuracy), test characteristics, and available data. It expressed the significant advantage of the proposed tests in formulating the new version, as is demonstrated in the following subsections.

A. Optimal truncation of the tests

In the absence of direct relationships between the test's parameters and the test's expenses and efficacy, for given D, α, β, it is possible to consider the following as the main test's efficacy factors:

- expected test time function (ETT) as a multiple of m_0;
- accumulated test truncation time (T^*_t/m_0) (maximum test duration) as a multiple of m_0;
- test truncation failure number (r_0).

The truncation selection is composed of two considerations:

a) In general, for sequential tests, as the truncation is heavier (lower max duration), the ETT is higher.
b) Optimal ratio between the max test duration and the max failure number permits heavy truncation without increasing the ETT function [17] [8].

In tests A, the ratio between the max test duration and the max failure number is not the optimal.

In tests C, the tests have very strong truncation while ETT is substantially higher than the non-truncated (Wald's [3]) tests.

In the proposed tests, the truncation is the heaviest without a significant increase of ETT (vs. the non-truncated). See Figs. 1 and 2. The advantage of the tests over the current ones regarding test time is illustrated (as an example) in Figs. 1 and 2 (tests A.8 and C.1 correspondingly). In order to permit a comparison between the tests by their time to decision, corresponding tests with the same true risks were designed.

In Fig. 1, the test truncation failure number (r_0) of the alternative test is better (7 vs. 8 of the standard's A.8), the maximum duration is also better (1.5% shorter) and still, its ETT is better. The ETT of test A.8 is 12% higher at the average vs. the ideal non-truncated test, while the proposed is only 6%.

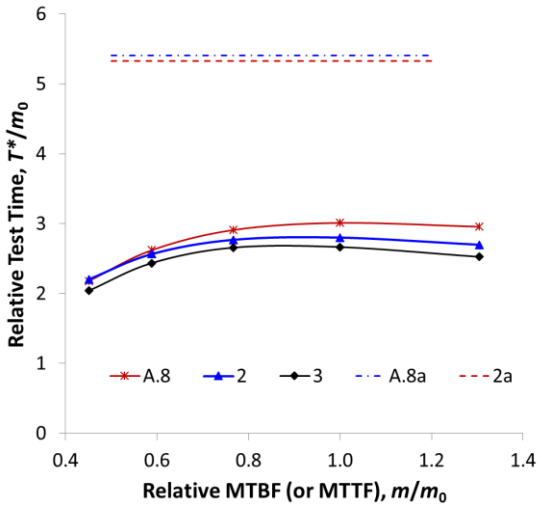

Figure 1. Expected test time and truncation time for A.8 and the alternative.
Test data: D=1.5, α=β=0.30 (nominal risks), α'=0.289 β'=0.363 (true risks for both tests).
A.8 – ETT (Expected accumulated test time to decision, T^*_e/m_0) of A.8;
2 – Ditto alternative;
3 – Ditto non-truncated test;
A.8a – Accumulated test truncation time (T^*_t/m_0) of A.8;
2a – Ditto alternative.

In Fig. 2, r_0 of the proposed test is 43 vs. 39 of the standard's C.1 (the maximum duration is slightly higher by 10%), but its ETT is much lower. The ETT of test C.1 is 41% higher at the average vs. the ideal non-truncated test, which

doubts the relevance of the test. The proposed test is very close to the ideal non-truncated test (only 10% higher at the average).

Examining all C tests vs. the proposed shows a 20% reduction of the ETT (at the average).

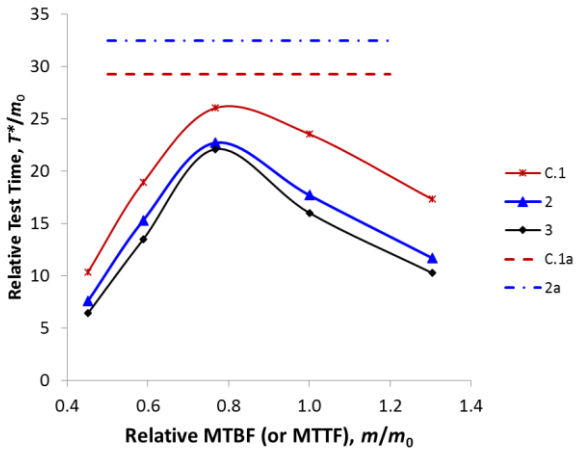

Figure 2. Expected test time and truncation time for C.1 and the proposed alternative.
Test data: D=1.7, α'=β'=0.050 (true risks).
C.1 – ETT (Expected accumulated test time to decision, T^*_e/m_0) of C.1, r_0=39;
2 – Ditto alternative, r_0=43;
3 – Ditto non-truncated test, r unlimited;
C.1a – Accumulated test truncation time (T^*_t/m_0) of C.1, r_0=39;
2a – Ditto alternative, r_0=43.

The advantage of the proposed tests (significantly truncated without significantly increasing the ETT vs. the non-truncated test) is achieved due to the optimal ratio between the test truncation failure number (r_0) and the accumulated test truncation time (T^*_t).

B. Range of the test parameters (variety of test plans, incl. interpolation)

The variety of "ready to use" tests in the current standard is very limited (17 total):

- Nine A tests that are restricted to equal nominal risks only (α=β).
- Eight C tests that are limited to D=1.7.

Additional A tests can be calculated by formulas (given in Annex E). The formulas result in substantial unknown deviations from the nominal risks and they do not carry out optimal truncation.

For additional C tests the standard refers to GOST R 27.402 [20].

- The GOST 27.402-95 includes 14 SPRT tests for D and α=β combinations.
- A method for additional test calculations is enclosed in Annex K of IEC-61124:
  - It consists of a complicated iterative procedure of finding values of four unknowns.
  - The end of the procedure is detected by an ambivalent variance of ETT function (change in the unknown values can lead to an increase of the ETT function on one side and a decrease on the other, so it is impossible to define an optimal test and its parameters).
  - No data is available regarding the optimal truncation (time and failure number) vs. the ETT function.

The proposed version includes 60 test plans that are "ready to use". It provides tests with a variety of risk values including several risk ratios (Table I), over few discrimination ratios: D = 1.5, 1.7, 2, 3, 5.

TABLE I. NOMINAL RISKS

α	0.05			0.1				0.2			0.3	0.4
β	0.05	0.1	0.2	0.05	0.1	0.2	0.4	0.05	0.1	0.2	0.3	0.1

Simple interpolation formulas for additional test plans are proposed. Using the formulas, it is possible to calculate test plans with intermediate parameter values with high accuracy (much more exact than in the standard's Annex E).

C. Risk accuracy

The sequential A test plans in the standard features two kinds of incorrectness regarding the test's risks:

- The true risks significantly deviate from the nominal (as seen in the standard's Table II)
- The "true" values declared in the standard's Table II are not accurate (the risks relative error is up to 104% when checked).

Detailed analysis of standard's 2nd edition (2006) is available in [17], and valid for the 3rd edition as well.

The standard's Type C plan features high accuracy of the risks.

In the proposed version, the true values are nominal (the average relative deviation is less than 0.002%).

D. Expected accumulated test time to decision (ETT)

- Type A plan's characteristics in the standard have substantial errors in the ETT (up to 17%) [17].
- In the current standard, the ETT is given by graphs (designated for each test plan). This approach is suitable only for a limited number of tests and is not necessary for practical use.
- The proposed test plans include five accurate values of ETT vs. m in the region between $m_1/D^{0.5}$ and $m_0*D^{0.5}$ (a constant step on a logarithmic scale). The given data is enough to restore the ETT function with high accuracy in this region. See Table II and Fig. 3.
- A spreadsheet (in accordance with Annex F of the standard) for generating the graphs and the other test characteristics (OC and boundaries) will be attached to the proposed version.

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- For any of the proposed test plans (see Table III), the ETT curve is defined via five points vs. the true *m* (MTBF or MTTF), and according to Table II:

TABLE II. ETT VS. TRUE *m* (MTBF OR MTTF)

m	$m_1/\sqrt{D}$	$m_1 = m_0/D$	$m_0/\sqrt{D}$	m_0	$m_0\sqrt{D}$
ETTj	ETT_L	ETT_1	ETT_M	ETT_0	ETT_H

Note: j = (L, 1, M, 0, H)

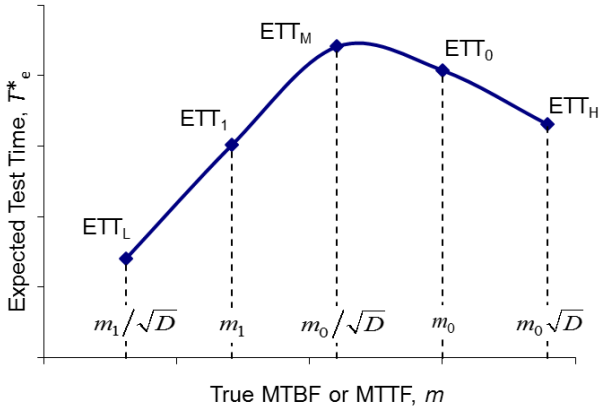

Figure 3. Example of the curve of expected test time to decision (ETT).

D. Operational characteristics (OC)

- In the current standard, the OC is given by graphs (designated for each test plan). This approach is suitable only for a limited number of tests and is not necessary for practical use.
- For the proposed test plans, the OC is in accordance to Wald's formulas as presented in Annex E.3.2 and Annex F.2.2 (for construction of the OC graph by spreadsheet program). The OC by Wald's formulas is accurate only for true risks (α' and β', see 4.3).

IV. PROPOSED TEST PLANS PRESENTATION

The proposed version includes 60 tests plans with all the required test data (boundaries and characteristics) in one table (see Table III).

The proposed changes can be implemented as follows:

- As an updated version of the standard in the part of sequential tests.
- Annex to the current standard, as an additional option for the sequential test plans.

V. CONCLUSION

The proposed version will be a significant improvement over the existing one. It is the result of development in the field of SPRT in recent years and the available computing power, which will support the requirements of today. It is both possible and necessary to conduct more economically efficient, more precise and more complex tests because of the accession of computer systems and stricter requirements in quality assurance and reliability. The changes will extend the use of SPRT and this standard.

The proposal for updating the standard has been accepted to the work-plan of Technical Committee TC-56 of International Electrotechnical Commission (IEC).

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This paper is dedicated to the bright memory of Eng. Eliezer Goldberg (1918–2015) in honor of his work over many years of phenomenal editing.

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ABBREVIATIONS

(The singular and plural of an abbreviation are always spelled the same)

ETT	expected accumulated test time to decision
MTBF	mean operating time between failures
MTTF	mean time to failure
OC	operating characteristic
SPRT	sequential probability ratio test

SYMBOLS

a	the accept line's intersection with the r axis
b	the accept and reject line's slope
b^*	$b^* = b \times m_0$, slope
c	the reject line's intersection with the r axis
D	discrimination ratio; $D=m_0/m_1$
m	true mean operating time between failures (MTBF) or mean time to failure (MTBF)
m_0	specified MTTF or MTBF (design goal)
m_1	lower limit for MTTF or MTBF
T^*_e	expected accumulated test time to decision (ETT)
T^*_t	accumulated test time stated as termination criterion (truncation or max duration)
r	observed number of failures during the test
r_0	test truncation failure number
α	nominal producer's risk (type I risk)
α'	true producer's risk
β	nominal consumer's risk (type II risk)
β'	true consumer's risk

TABLE III. EXAMPLE FOR SEQUENTIAL TEST PLANS

D, b^*	α' %	β' %	a	c	T^*_t/m_0	r_0	ETT_L	ETT_1	ETT_M	ETT_0	ETT_H
D=1.5 b^*=1.2333	5	5	-8.070	7.905	63.93	78	13.6	27.0	40.8	30.5	19.3
	5	10	-6.465	8.054	48.37	60	13.8	24.8	31.8	23.7	15.4
	5	20	-4.455	7.506	36.22	46	12.5	19.5	21.5	15.8	10.5
	10	5	-8.137	6.395	48.69	58	11.1	21.3	32.1	27.9	19.2
	10	10	-6.209	6.054	37.96	46	10.4	18.3	24.2	20.6	14.5
	10	20	-4.476	5.960	24.97	31	9.8	14.5	16.4	13.8	10.3
	10	40	-2.455	4.593	13.70	18	6.3	7.6	7.7	6.6	5.3
	20	5	-7.516	4.296	37.39	43	7.6	14.2	21.8	21.9	17.0
	20	10	-5.811	4.361	25.92	30	7.5	12.4	16.4	16.0	12.8
	20	20	-3.980	3.921	16.09	19	6.3	8.8	10.2	9.8	8.3
	30	30	-2.320	2.354	6.44	7	3.0	3.5	3.9	3.9	3.7
	40	10	-4.902	2.260	14.26	15	4.0	6.0	7.9	8.8	8.6

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